VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

IBRAHIMBAGH, HYDERABAD - 500031.

Approved by A.I.C.T.E., New Delhi and

Affiliated to Osmania University, Hyderabad-07

Sponsored by

VASAVI ACADEMY OF EDUCATION

Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR

M.E. (ECE) Embedded Systems and VLSI Design

With effect from 2018-2019

(For the batch admitted in 2018-19)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

DEPARTMENTOF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION FOR

M.E (ECE) EMBEDDED SYSTEMS AND VLSI DESIGN

I-SEMESTER w.e.f. 2018-19 under CBCS

S.No	Course code	Course Title	Scheme of Instruction			Scheme of Examination			Total	Credits
			L	T	P	Duration in Hrs	CIE	SEE		
	Theory									
1.	PI18AC110EH	Audit course-I: English for Research Paper Writing	2	-	-	3	40	60	100	-
2.	PI18PC110EC	Core - I: Embedded Systems Design	3	-	-	3	40	60	100	3
3.	PI18PC120EC	Core - II: Digital IC Design	3	-	-	3	40	60	100	3
4.	PI18PC130EC	Core - III: Analog IC Design	3	-	-	3	40	60	100	3
5.	PI18PE1X0EC	Professional Elective - I	3	-	-	3	40	60	100	3
6.	PI18PE1X0EC	Professional Elective - II	3	-	-	3	40	60	100	3
7.	PI18PE1X0EC	Professional Elective - III	3	-	-	3	40	60	100	3
	Laboratory									
8.	PI18PC111EC	Design and Simulation Laboratory - I	-	-	3	-	50	-	50	1.5
9.	PI18PC121EC	Embedded Systems Laboratory	-	-	3	-	50	-	50	1.5
10.	PI18PC118EC	Seminar – I	-	-	2	-	50	-	50	1
			20	**-**	**8**	**-**	**430**	**420**	**850**	**22**

S.No.	Course Code	Course	Hours per week
Professional Core Courses			
1.	PI18PC240ME	Research Methodology and IPR	2
2.	PI18PC110EC	**Core – I:** Embedded Systems Design	3
3.	PI18PC120EC	**Core – II:** Digital IC Design	3
4.	PI18PC130EC	**Core – III:** Analog IC Design	3
5.	PI18PC210EC	**Core – IV:** Embedded Real Time Operating Systems	3
6.	PI18PC220EC	**Core – V:** Mixed Signal IC Design	3
7.	PI18PC230EC	**Core – VI:** Physics of Semiconductor Devices	3
8.	PI18PC111EC	Design and Simulation Laboratory-I	3
9.	PI18PC121EC	Embedded Systems Laboratory	3
10.	PI18PC211EC	Design and Simulation Laboratory –II	3
11.	PI18PC212EC	Embedded Systems Application Laboratory	3
12.	PI18PW219EC	Mini Project	2
13.	PI18HS200EH	Skill Development Course	2
14.	PI18PC118EC	Seminar – I	2
15.	PI18PC218EC	Seminar – II	2
16.	PI18PW319EC	Dissertation-Phase-I / Internship	8
17.	PI18PW419EC	Dissertation-Phase-II / Internship	24
Professional Electives			
Elective – I			
18.	PI18PE110EC	Advanced Computer Organization	3
	PI18PE120EC	System on Chip Architecture	3
	PI18PE130EC	Electromagnetic Interference & Compatibility	3
Elective – II			
19.	PI18PE140EC	VLSI Technology	3
	PI18PE150EC	System Design and Reliability	3
	PI18PE160EC	Reconfigurable System Design	3
Elective – III			
20.	PI18PE170EC	VLSI Physical Design	3
	PI18PE180EC	Hardware-Software Co-design	3
	PI18PE190EC	Scripting Languages for Embedded Systems	3
Elective – IV			
21.	PI18PE210EC	Low Power VLSI Design	3
	PI18PE220EC	Principles of VLSI System Design	3
	PI18PE230EC	Low Power Embedded Systems Design	3
Elective – V			
22.	PI18PE240EC	CPLD & FPGA Architectures and Applications	3
	PI18PE250EC	MEMS	3
	PI18PE260EC	RFIC Design	3
Elective – VI			
23.	PI18PE310EC	Design for Testability	3
	PI18PE320EC	Integrated Optics & Photonic Systems	3
	PI18PE330EC	High Level Synthesis	3
Audit Course – I			
24.	PI18AC110EH	English for Research Paper Writing	2
	PI18AC120XX	Value Education	2
	PI18AC130XX	Stress Management by Yoga	2
	PI18AC140XX	Sanskrit for Technical Knowledge	2
Audit Course –II			
25.	PI18AC210EH	Pedagogy Studies	2
	PI18AC220XX	Personality Development through Life Enlightenment Skills.	2
	PI18AC230XX	Constitution of India	2
	PI18AC240XX	Disaster Management	2
Open Electives			
26.	PI18OE310XX	Business Analytics	3
	PI18OE320XX	Industrial Safety	3
	PI18OE330XX	Operations Research	3
	PI18OE340XX	Cost Management of Engineering Projects	3
	PI18OE350XX	Composite Materials	3
	PI18OE360XX	Waste to Energy	3

DEPARTMENT OF HUMANITIES AND SOCIAL SCIENCES
SYLLABUS FOR M.E. (ECE) – I SEMESTER
ENGLISH FOR RESEARCH PAPER WRITING

Instruction: 2 Hours**/** week	**Semester End Exam Marks: 60**	**Course Code: PI18AC110EH**
Credits: NIL	CIE Marks : 40	Duration of SEE: 3 Hours

Course Objectives	**Course Outcomes**
Students Should be able to	At the end of the course, students will be able to
• Understand that how to improve your writing skills and level of readability • Learn about what to write in each section • Understand the skills needed when writing a Title	• write research papers • write citations as per the MLA style sheet and APA format • write concisely and clearly following the rules of simple grammar, diction and coherence.

Unit-I: Planning and Preparation, Word Order, Breaking up long sentences. Structuring Paragraphs and Sentences, Being concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit-II: Clarifying Who Did What, Highlighting your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

Unit-III: Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit-IV: Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, useful phrases, how to ensure paper is as good as it could possibly be the first-time submission.

Unit-V: Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

LEARNING RESOURCES :

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER
EMBEDDED SYSTEMS DESIGN

Course Code : **PI18PC110EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Implement embedded hardware & firmware using embedded-C for C51 to interface with different I/O. 2. Demonstrate the embedded system design using ARM IP core with emphasis on its programming model. 3. Interpret serial and parallel bus communication protocols used for providing connectivity and propose debugging techniques for testing.	**At the end of the course, students will be able to:** 1. Define, Classify and Analyze embedded system product design with IC Technology. 2. Design & implement device drivers in embedded-C for C51 target MCU to interface I/O. 3. Analyze ARM IP Core usage in design with its programming model. 4. Justify the hardware software co-design issues along with debugging techniques. 5. Propose serial & parallel protocols to design networked embedded systems.

UNIT – I
Embedded Systems Overview: Definition of Embedded System; Examples; Design Challenges–Optimizing Design Metrics; Selection of processor or controller & memories; Processor Technology; RISC Vs CISC

UNIT – II
Real World Interfacing using Embedded C with AT89S52 (8051 Microcontroller): ADC0808, LED, Seven Segment Displays, DAC, LCD, Keypad, RTC, DC Motor, Stepper Motor driving actuators using PWM.

UNIT – III
ARM Core Architecture: Introduction to RISC concepts with ARM as CPU, ARM engine Architecture, AMBA Bus, Core Registers, Programming Modes, Importance of Thumb Mode, CPSR, SPSR, Pipeline, Exceptions, Interrupts and vector table; ARM Programming Model; Core Extensions, ARM Revisions, ARM processor families and comparisons.

UNIT – IV
Embedded Networking: Serial protocols topology & working principles and frame formats – I^2C; SPI; USB; CAN; Ethernet; Parallel Protocols – PCI; PCIx; AMBA bus

UNIT – V
Embedded Debugging Techniques: Debugging Methods using Software and Hardware; usage of JTAG adaptor for ARM and Embedded ICE Embedded Software Architectures Introduction: Round-Robin; RR with Interrupt; Functional Queue Scheduling & need of RTOS

Suggested Reading:

1. Frank Vahid, Tony Givargis "Embedded System Design – A Unified Hardware/Software Introduction" John Wiley & Sons, Inc. 2002.
2. Andrew N Sloss, Dominic Symes & Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", The Morgan Kaufmann Series 2004.
3. Mazidi M.A and Mazidi J.G, "The 8051 Microcontroller and Embedded Systems", Pearson 2007.
4. David E Simon, "An Embedded Software Primer", Pearson Education, 2005.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Digital IC Design

Course Code : **PI18PC120EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Appreciate the importance of secondary effects such as velocity saturation, sub-threshold leakage of MOSFETS and study the modifications in the device models in DSM regime. 2. Analyse the effect of sizing the devices on CMOS inverter performance the inverters, 3. Optimize critical data paths considering Logical, Electrical and Branch Efforts 4. Estimate power and delay in both static and dynamic CMOS combinational and sequential circuits 5. Design arithmetic building blocks and memory blocks for use in a microprocessor and analyse their performance.	**At the end of the course, students will be able to:** 1. Appreciate the secondary effects of MOSFETS in DSM regime , perform timing analysis and size the inverters for optimum path delay, 2. Perform path optimization of CMOS gates with Logical Effort, 3. Compute delay and power dissipation in both dynamic and static CMOS designs, and apply pipelining techniques to optimize Sequential Circuits 4. Analyse the interconnect parasitics and their effect on clock distribution 5. Design a simple datapath for a processor and apply power reduction techniques 6. Design a 6T SRAM cell and organise a memory bank

UNIT – I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, MOSFET secondary effects, Simple Interconnect Wire models, Design rules, Sub-threshold Conduction. CMOS Inverter – Static and Dynamic Behaviour, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis, Detailed Load Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

UNIT – II

Designing Combinational Logic in CMOS: Static CMOS design: Complimentary CMOS, Ratioed Logic, Pass Transistor Logic, Transmission Gate Logic, Optimizing Paths with Logical effort.
Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic, Signal Integrity Issues, Cascading Dynamic Gates

UNIT – III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles, Pipelining to optimize Sequential Circuits, Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic, Advanced Interconnect Techniques, Power Grid and Clock design: Power Distribution Design, Clocking and Timing Issues, Phase-Locked Loops / Delay Locked Loops.

UNIT – IV

Designing Arithmetic Building Blocks: Datapaths in Digital Processor Architectures,: The Adder, The Multiplier, The Shifter and The Comparator. Power and Speed Trade offs in Datapath Operators: Design-Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues

UNIT – V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, SRAM Cell Layout

Topics beyond syllabus

*Advanced Topics in Memory Design: Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies, PLLS and DLLs

Suggested Reading:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective"", Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in DSM Technology", 3rd Edition, Tata McGraw Hill, 2008.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Analog IC Design

Course Code : **PI18PC130EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Realize that ICs are similar to discrete component circuits with special constraints. 2. aexposed to these constraints and make them design the ICs. 3. Capable of arriving at a suitable architecture, for a given function, which can be realized in IC form	**At the end of the course, students will be able to:** 1. Apply mathematics and physics to model analog circuits. 2. Arrive at an optimum solution to a problem in analog circuits domain. 3. Design simple CMOS analog circuits and analyse of their performance 4. Design and analyse the performance of Operational amplifiers

UNIT – 1

Introduction: What are electronic devices and circuits – Types of electrical signals – Characteristics of analog signals – Analog functions – Devices characteristics needed to perform these functions. Discrete component approach to analog circuit – Integrated circuit approach, silicon as base material. Integrated circuit – Components for Ics – Resistors, Capacitors, inductors diodes, BJTS, MOSFETS – Their IC architectures, limitations, circuits design philosophies – Different families of circuits device models. Basic analog circuits – Amplifiers – Different type of loads – Biasing techniques – current mirrors – Coupling techniques between stages.

UNIT – II

Biasing techniques: Basic current mirror architecture – Specifications of current mirrors – Cascode current mirrors – Wide swing current mirrors Wilson current mirror – Degenerate current sources – peaking current sources for very low current biasing – enhanced output impedance current mirrors, Sensitivity analysis of current. Mirrors: Voltage references – VBE, VT and Zenner diode based references, Band gap reference

UNIT – III

Single stage amplifiers CS, CG, CD amplifiers with resistive, diode, current source, and current mirror loads – performance analysis of these circuits – input, output, current and voltage gains at low frequencies swing, frequency response and phase response of these amplifiers, Multistage amplifiers and biasing and swing problems. Cascode amplifiers – Folded cascade amplifiers – Swing analysis. Differential amplifiers, biasing and analysis of performance, Specifications – common and differential mode gain – common mode rejection ratio power rejection ratio, swing differential input differential output amplifier, differential input single ended output amplifier variable gain amplifiers Noise in amplifiers.

UNIT – IV

Operational amplifiers – characteristics and specifications – Two and three stage Op-Amps – analysis of gain, frequency and phase response – Coupling problems, fully differential amplifiers – Cacodes, folded 6ascades – common mode feedback, and circuits, active cascade Op-Amp – current differential amplifiers – current feedback Op-Amps, - Gilbert Cells. OTAS.

UNIT – V

Oscillators and mixers: Basics of oscillators – Feedback oscillators, negative resistance oscillators, (two port oscillators), ring oscillators – Differential ring oscillators, LC oscillators, relaxation oscillators, voltage controlled oscillators, Tuning delay and frequency. Diode based mixers, Gilbert cell based mixers.

Suggested reading:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Advanced Computer Organization

Course Code : **PI18PE110EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Advanced computing/processing system includes several functional aspects like processing, memory, high speed logic, industry standard interfaces and so on. The major objective of this course is to combine all these functional aspects and develop a processing system for the given specifications.	**At the end of the course, students will be able to:** 1. Evaluate the performance parameters of advanced processors, analyse and compare advantages, limitations and applications of advanced processors. 2. Design the data path and control unit for the given specifications and analyze different control unit design approaches. 3. Demonstrate the knowledge of issues involved in memory organization. 4. Analyze various input-output techniques for proper transfer of data between CPU and different peripheral devices. 5. Use modern EDA tools for solving advanced processing system related problems. 6. Become acquainted with recent advancements in the area of advanced processing systems.

UNIT – I

Review of Computer Arithmetic, Application Processing Unit , A Note on the ARM Model, Standard Processor and processing system, Processor Design Techniques: Instruction Pipelining, Super Scalar techniques, Super scalar and super pipeline design, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

UNIT – II

Control Unit Design approaches, Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Processor Selection Criteria, Case studies on MicroBlaze Processor, Discrete FPGA-Processor

UNIT – III

Memory Organization: the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT – IV

I-O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Synchronous bus and asynchronous bus, IO Processor, General Purpose Input/Output ,Communications Interfaces,Programmable Logic Interfaces, AXI Standard, AXI Interconnects and Interfaces, Processing System External Interfaces

UNIT – V

Parallel Computer Systems: Instruction Level Parallelism (ILP) , Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors, SIMD computers and Super computers, High Performance Computing(HPC), Case study on advanced processing system, An Overview of HPC Applications

Suggested Reading:

1. William Stallings, Computer Organization and Architecture designing for Performance, 7th edition, PHI, 2007.
2. Carl Hamacher, Vranesic, Zaky, Computer Organization, 5th edition, MGH.
3. Hayes John P; Computer Architecture and organization; 3rd Edition, MGH, 1998.
4. John L. Hennessy and David A. Patterson, Computer Architecture – A quantitative Approach, 3rd Edition, Elsevier, 2005.
5. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

System on Chip Architecture

Course Code : **PI18PE120EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. To understand hardware design. 2. To classify data types. 3. To apply hardware system prototyping tools. 4. To acquire the knowledge of arm system control processor. 5. To design system in package.	**At the end of the course, students will be able to:** 1. design system in package. 2. apply hardware system prototyping tools.. 3. classify data types. 4. Design Arm MMU architecture. 5. Model arm system control processor.

UNIT – I

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor, Processor design trade off, Design for low power consumption. ARM Processor as System-on- Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface.

UNIT – II

ARM Assembly Language Programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions. Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

UNIT – III

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design- an example – memory management.
Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

UNIT – IV

Architectural Support for Operating System: An introduction to Operating Systems – ARM System control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output.

UNIT – V

System in Package Design: Advantages and disadvantages between SoC, SiC and board level design; SiP Design flow, System Planning, Chip-Package co-design, System Optimization; SiP Design Layout, Simulation, Verification; Gaps in SiP Design, Power optimization tools, Parasitic extraction tools, Signal Integrity.
Examples of SiP.

Suggested Reading:

1. Steve Furber, ARM System on Chip Architecture, 2nd ed., Addison Wesley Professional, 2000.
2. Ricardo Reis, Design of System on a Chip: Devices and Components, 1st ed., Springer, 2004.
3. Jason Andrews, Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) , BK and CDROM.
4. Prakash Rashinkar, System on Chip Verification – Methodologies and Techniques, Peter Paterson and Leena Singh L ,Kluwer Academic Publishers, 2001.
5. System in Package (SiP) – A review, Technical Review-I, R&D Cell, Vasavi College of Engineering, Ibrahimbagh, Hyderabad, Telangana.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Electromagnetic Interference & Compatibility

Course Code : **PI18PE130EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT – I

Introduction and Sources of EMI: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT – II

Types of Electromagnetic Coupling:Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near78 Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT – III

EMI Measurements: EMI Shielded Chamber, Open Area Test Site, TEM Cell, GTEM cell Sensors/ Injectors/ Couplers, LISN, voltage probe, Current probe Test beds for ESD and EFT.

UNIT – IV

EMI Mitigation Techniques: Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT – V

EMC System Design: PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Suggested Reading:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996
2. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", 2nd Edition, John Wiley and Sons, NewYork. 1988.
3. C.R.Paul, "Introduction to Electromagnetic Compatibility", John Wiley and Sons, Inc, 2006.
4. Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

VLSI Technology

Course Code : **PI18PE140EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Impart a knowledge about VLSI Integrated circuits their structures, evolution and benefits of these circuits in realizing complex electronics functions to students. 2. Impart knowledge about IC fabrication technologies and their advancement over time. 3. Impart knowledge about the sub process technologies that are involved in IC fabrication and how they are put together to form complete fabrication process. 4. Acquaint the students about clean room environments needed for IC fabrication and their importance. 5. Impart knowledge about complex process of VLSI packaging and testing and their advancements.	**At the end of the course, students will be able to:** 1. Describe evolution and progress of VLSI technology, Electronic functions and basic device structures on Integrated circuits. 2. Apply alternate technologies and Process flows for realization of VLSI chips 3. Demonstrate Unit processes involved in VLSI technology such as silicon wafer preparation, epitaxy, oxidation and diffusion, lithography, etching, implantation etc. 4. Specify Other unit processes involved in VLSI technology such as deposition, lithography and etching 5. Specify Clean Room environments needed for VLSI processing and packaging and testing of the VLSI chips.

UNIT – I

Introduction – Integrated Circuits Review of history of VLSI technology progress–. Electronic Functions – Components – Analog and Digital ICs. Basic Devices in ICs – Structures Resistors – Capacitors – Inductors. Diodes – Bipolar Junction Transistors – Field Effect Transistors. Isolation techniques in MOS and bipolar technologies.

UNIT – II

Monolithic ICs – Silicon as the Base Material and its advantages, various Layers of ICs – Substrate – Active Layer -Oxide/Nitride Layers – Metal/Poly Silicon Layers – Functions of Each of the Layers. Process Flow for Realization of Devices. Description of Process Flow for Typical Devices viz., FET and BJT.

UNIT – III

Silicon Wafer Preparation – Electronic Grade Silicon – CZ and FZ Methods of Single Crystal Growth – Silicon Shaping – Mechanical Operations, Chemical Operations – Prefabrication Processes.
Epitaxy: Growth Dynamics – Process Steps. Vapour phase, Solid phase and Molecular Beam Epitaxial Processes. Epitaxial Reactors.
Oxide Growth: Structure of SiO_2, Growth Mechanism and Dynamics – Oxide Growth by Thermal method.

UNIT – IV

Deposition techniques Chemical Vapour Deposition (CVD) and associated methods like LPCVD and PECVD. PVD thermal evaporation and sputtering. Step coverage issues.
Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their characteristics, optical exposure systems contact and projection systems, steppers, X-ray – Electron Beam Lithography.
Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT – V

Ion implantation: Range and Penetration Depth – Damage and Annealing – Ion Implantation machine.
Diffusion: Constant and Infinite Source Diffusions – Diffusion Profiles – Diffusion Systems – Multiple Diffusions and Junction Formations. Packaging: die and Bonding and Packaging, Testing. Clean rooms and their importance in VLSI technology

Suggested Reading:

1. S.M. Sze, VLSI Technology, Mc Grawhill International Editions.
2. CY Chang and S.M. SZe , VLSI Technology, Tata Mc Graw-Hill Companies Inc.
3. J.D. Plummer, M.D. Deal and P.B. Griffin ,The Silicon VLSI Technology Fundamentals, Practice and modeling, Pearson Education 2009
4. Stephen A, The Science and Engineering of Microelectronic Fabrication, Campbell Oxford 2001.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

System Design and Reliability

Course Code : **PI18PE150EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT – I

System design aspects- Structure of systems in general-hardware, software components, testability of systems, and design of systems from testability point of view.

UNIT – II

System Reliability: Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces. Test environments, testing for reliability and durability, failure reporting,

UNIT – III

Concepts of MTBF Maintainability and Availability. Maintainability and its equation. Factors Affecting maintainability. Measures of, Maintainability, Mean Down Time, Availability Intrinsic availability equipment availability & Mission availability. Replacement processes and Policies.

UNIT – IV

Reliability of electronic components, component types and failure mechanisms,: Evaluation of reliability of electronic components like integrated circuits. Life cycle of electronic components, bath tub curve. Accelerated life tests for components, reliability screening procedures, burn in test. Standards for reliability evaluation and screening at component level.

UNIT – V

System level reliability testing, - Reliability evaluation and screening procedures at system level. Life tests for systems, accelerated testing reliability costs, Standards for system level reliability evaluation and screening.

Suggested Reading:

1. Kailash C. Kapur, Michael Pecht, Reliability Engineering, Wiley, 2014.
2. Patrick D.T. O' Connor, David Newton and Richard Bromley, Practical Reliability Engineering, 4/e , John Wiley & Sons, 2002.
3. Elmer Eugene Lewis, Introduction to Reliability Engineering, 2/e, Wiley International, 1996.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Reconfigurable System Design

Course Code : **PI18PE160EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT - I

Introduction: Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

UNIT - II

Parallel and Advanced Processors: Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

UNIT - III

Reconfigurable Architectures: FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

UNIT - IV

Reconfiguration Management : Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time

UNIT - V

Case Studies of FPGA Applications: Dynamic Partial Reconfigurable FIR Filter Design, Trigonometric Computing, Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip, A Fast Run Time Reconfigurable Platform for Image Edge Detection, Efficient Floating-Point Implementation of High-Order (N) LMS Adaptive Filters in FPGA, Area/Performance Improvement of NoC Architectures.

Suggested Reading:

1. Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007
2. Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA based Computation", Elseiver 2008
3. Niccolo Battezzatti, Luca Sterpone, Massimo Violante, "Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications", Springer 2011.
4. Kai Hwang, "Advanced computer architecture – Parallelism, Scalability, Programmability"; Tata McGraw Hill Publishing company Ltd., New Delhi, 1993.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

VLSI Physical Design

Course Code : **PI18PE170EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. To understand the structures of different components of VLSI design. 2. To draw stick and layout diagrams of circuits. 3. To apply design rules to layouts. 4. To acquire the knowledge cell based designs. 5. To understand circuit parameters of extracted physical layouts.	**At the end of the course, students will be able to:** 1. Design the structures of different components of VLSI design. 2. Apply the basic concepts of physical design to layouts and stick diagrams. 3. Apply Design rules for layouts of circuits. 4. Design hierarchical circuit Layouts using cell concepts. 5. Model and extract circuit parameters from physical layout using CAD tools.

UNIT – I

Scope of physical design – Components of VLSI – Various layers of VLSI – Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, Diodes, cost and performance analysis.

UNIT – II

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Diodes. Parasitics – latch up and its prevention. Device matching and common centroid techniques for analog circuits

UNIT – III

Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and their effects, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT – IV

Cell concepts – cell based layout design – Wein-berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. Large scale physical design, interconnect delay modeling, floor planning, placement, routing and clock distribution.

UNIT – V

CAD Tools: Layout editors, Design rule checkers, circuit extractors – Hierarchical circuit extractors – Automatic layout tools, silicon compilers, modeling and extraction of circuit parameters from physical layout.

Suggested Reading:

1. Preas, M. Lorenzatti, "Physical Design and Automation of VLSI Systems", The Benjamin-Cummins Publishers, 1998.
2. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
3. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
4. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Hardware-Software Co-design

Course Code : **PI18PE180EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level
specification languages, Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Suggested Reading:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Scripting Languages for Embedded Systems

Course Code : **PI18PE190EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. To understand control structures of perl. 2. To classify character classes. 3. To apply subroutines and data structures. 4. To acquire the knowledge extending perl. 5. To understand broad features of SKILL, CGI.	**At the end of the course, students will be able to:** 1. Design control structures of perl. 2. Apply subroutines and data structures. 3. Extend perl to embedding perl. 4. classify character classes. 5. Model features of SKILL, CGI.

UNIT – I

Overview of scripting languages-PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT – II

Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT – III

Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions.
Inter process communication,- signals, files, pipes, sockets,.

UNIT – IV

Threads- process model, thread model, Perl debugger- using debugger commands, customization, internals and externals, internal data types, extending Perl, embedding Perl, exercises for programming using Perl.

UNIT – V

Other languages: Broad features of other scripting languages SKILL, CGI, java script, VB script.

Suggested Reading:

1. Larry Wall, Tom Christiansen, John Orwant, "programming perl", oreilly publications, 3rd edition.
2. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly publications.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Design and Simulation Laboratory-I

Course Code : **PI18PC111EC**	Instruction : 3 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1.5

Course Objectives	Course Outcomes
1. To provide an introduction to fundamentals of computer aided design tools for the modeling, design, analysis, test and verification of digital integrated circuit or systems.	**At the end of the course, students will be able to:** 1. Familiarize with frontend CAD tools to design digital integrated circuits. 2. Develop Verilog / VHDL for combinational logic circuits in various level of abstraction. 3. Develop Verilog / VHDL for sequential logic circuits in various level of abstraction 4. Write test bench in HDL to verify digital logic circuits 5. Synthesize and verify the digital logic circuits on FPGA

Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Design and simulation of combinational circuits

(ii) Design and simulation of sequential circuits

(iii) Design and simulation of mixed signal circuits

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Embedded Systems Laboratory

Course Code : **PI18PC121EC**	Instruction : 3 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1.5

Course Objectives	Course Outcomes
1. Compare different cross compilers and install Keil v5 µVision IDE in x86 Windows 7 & above or Linux 2.6 (Ubuntu 16.04 LTS) & above host. 2. Simulate actual hardware environment by designing hardware in Proteus7.x & above. 3. Implement Device Drivers for off-chip I/O & memories with C51 MCU.	**At the end of the course, students will be able to:** 1. Implement embedded C constructs to configure built-in registers of C51 target. 2. Demonstrate the hardware emulation of the design on Proteus 7.x IDE. 3. Design & Implement off-chip OS-less device drivers for C51 in Keil v5 µVision IDE 4. Demonstrate efficient Interrupt Service Routine coding principles in C/C++. 5. Analyze & suggest debugging methods for any given specifications with C51 target.

List of Experiments using Embedded C/Embedded C++:

1. To toggle LEDs connected to GPIOs of AT89S52 with some intentional Delay.
2. To design & implement 4x3 matrix Keypad Device Driver for ASCII mapping.
3. To design & implement 2x16 LCD Device Driver for displaying below text:

   Line-1: "**Welcome@ESD Lab!**"

   Line-2:"**Enter to Proceed**"
4. To Configure Timer0 and Timer1 for intended delay without interrupts.
5. To design & demonstrate the UART drivers for data transmission and data reception at 9600bps full duplex baud.
6. To design & implement the concept of writing Interrupt Service Routine (ISR) for external interrupt INT0, INT1.
7. To design & implement the concept of mixing of external ISRs with Internal ISRs and understanding the ISR handling process.
8. To design & implement LED Seven Segment driver with adjustable delay.
9. To design & implement User Centric template Menu designs in Embedded C
10. To design and implement embedded C/C++ constructs for programming LPC2148 ARM powered MCU.
11. Mini project based on C51 or LPC2148 target and its execution.

Suggested tools for use:

1. Hardware Target CPU – AT89S52 ; LPC2148 (ARM7 TDMI-S)
2. Embedded Software Development – Keil µVision5 IDE
3. Embedded Debugger – Keil µVision5 Debugger
4. Hardware Simulator – Proteus

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – I SEMESTER

Seminar – I

Course Code : **PI18PC118EC**	Instruction : 2 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1

Course Objectives	Course Outcomes
1. Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	**At the end of the course, students will be able to:** 1. Selection of a suitable topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of seminar report.

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Embedded Systems, VLSI Design and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

DEPARTMENTOF ELECTRONICS AND COMMUNICATIONS ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION FOR
M.E (ECE) EMBEDDED SYSTEMS AND VLSI DESIGN
II-SEMESTER w.e.f. 2018-19 under CBCS

S. No	Category	Course code	Course Title	Scheme of Instruction			Scheme of Examination			Total	Credits
				L	T	P	Duration in Hrs	CIE	SEE		
Theory											
1.	AC	PI18AC210EH	Audit course-II: : Pedagogy Studies	2	-	-	3	40	60	100	-
2.	PC	PI18PC240ME	Research Methodology and IPR	2	-	-	3	40	60	100	2
3.	HS	PI18HS200EH	Skill Development Course	2	-	-	3	40	60	100	2
4.	PC	PI18PC210EC	**Core–IV:** Embedded Real Time Operating Systems	3	-	-	3	40	60	100	3
5.	PC	PI18PC220EC	**Core – V:** Mixed Signal IC Design	3	-	-	3	40	60	100	3
6.	PC	PI18PC230EC	**Core – VI :** Physics of Semiconductor Devices	3	-	-	3	40	60	100	3
7.	PE	PI18PE2X0EC	Professional Elective - IV	3	-	-	3	40	60	100	3
8.	PE	PI18PE2X0EC	Professional Elective - V	3	-	-	3	40	60	100	3
		Laboratory									
9.	PC	PI18PC211EC	Design and Simulation Laboratory –II	-	-	3	-	50	-	50	1.5
10.	PC	PI18PC212EC	Embedded Systems Application Laboratory	-	-	3	-	50	-	50	1.5
11.	PW	PI18PW219EC	Mini Project	-	-	2	-	50	-	50	1
12.	PC	PI18PC218EC	Seminar – II	-	-	2	-	50	-	50	1
				21	**-**	**10**	**-**	**520**	**480**	**1000**	**24**

DEAPRTMENT OF HUMANITIES AND SOCIAL SCIENCES
SYLLABUS FOR M.E. (ECE) – II SEMESTER
PEDAGOGY STUDIES
VASAVI COLLEGE OF ENGINEERING(AUTONOMOUS)

Instruction: 2 Hours/ week	Semester End Exam Marks: 60	Course Code: PI18PC210EH
Credits: 0	CIE marks: 40	Duration of SEE: 3 hrs.

Course Objectives	Course Outcomes
Students will be able to: 1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. 2. Identify critical evidence gaps to guide the development.	**Students will be able to understand:** 1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries? 2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners? 3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit-I **Introduction and Methodology :**
- Aims and rationale, Policy background, Conceptual framework and terminology
- Theories of learning, Curriculum, Teacher education.
- Conceptual framework, Research questions.
- Overview of methodology and Searching.

Unit-II
- **Thematic overview:**
  - Pedagogical practices that are being used by teachers
  - in formal and informal classrooms in developing countries.
  - Curriculum, Teacher education.

Unit-III
- **Evidence on the effectiveness of pedagogical practices**
  - Methodology for the in depth stage: quality assessment of included studies.
  - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?
  - Theory of change.
  - Strength and nature of the body of evidence for effective pedagogical practices.
  - Pedagogic theory and pedagogical approaches.
  - Teachers' attitudes and beliefs and Pedagogic strategies.

Unit-IV
- **Professional development: alignment with classroom practices and follow-up support**
  - Peer support
  - Support from the head teacher and the community.
  - Curriculum and assessment
  - Barriers to learning: limited resources and large class sizes

Unit-V
- **Research gaps and future directions**
  - Research design
  - Contexts
  - Pedagogy
  - Teacher education
  - Curriculum and assessment
  - Dissemination and research impact.

Suggested reading

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

DEPARTMENT OF MECHANICAL ENGINEERING
SYLLABUS FOR M.E (ECE) II-SEMESTER
RESEARCH METHODOLOGY AND IPR

Instruction: 2 Hours/ week	Semester End Exam Marks: 60	Course Code: PI18PC240ME
Credits: 2	Sessional Marks: 40	Duration of Semester End Exam: 3 hrs.

Course Outcomes

At the end of the course, Students will be able to

- Understand research problem formulation.
- Analyze research related information and follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II

Effective literature studies approaches, analysis Plagiarism, Research ethics,

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
5. Mayall, "Industrial Design", McGraw Hill, 1992.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DEPARTMENT OF HUMANITIES AND SOCIAL SCIENCES
SYLLABUS FOR M.E. (ECE) – II SEMESTER
SKILL DEVELOPMENT COURSE

Instruction: 2 Hours/ week	Semester End Exam Marks: 60	Course Code: PI18HS200EH
Credits: 2	CIE Marks : 40	Duration of SEE: 3 Hours

Course Objectives	Course Outcomes
Students Should be able to: The four major skills of language learning, listening, speaking, reading and writing provide the right key to success. The main objective of the Skill Development Course curriculum is to involve content for all the above mentioned four skills in teaching English and to get students proficient in both receptive and productive skills.	At the end of the course, students will be able to • Better Comprehension and Presentation Skills • Exposure to Versant, AMCAT and better strike rate during placement • Better Interview Performance

Unit I: **Remedial English: Delightful Descriptions**:
Describing Past, Present and Future Events.

Unit II: **Developing Conversational Skills –** Exchange of pleasantries, Exchange facts and opinions, Using relevant vocabulary.

UNIT III: **Contextual Conversations:** Ask for Information, Give Information, Convey bad news, show appreciation

UNIT IV: **Business English**: **Professional Communication**:
Concise Cogent Communication, Active Listening, Interact, Interpret and Respond. **Expositions and Discussions:** Organization, Key Points, Differing Opinions, Logical conclusions. **Effective Writing Skills:** Structure, Rough Draft, Improvisations and Final Draft for Emails, paragraphs and Essays. **High Impact Presentations:** Structure, Content, Review, Delivery

Unit V: **Industry Orientation and Interview Preparation**
Interview Preparation– Fundamental Principles of Interviewing, Resume Preparation, Types of Interviews, General Preparations for an Interview. **Corporate Survival skills**: Personal accountability, Goal Setting, Business Etiquette, Team Work

Suggested Readings:

1. Business Communication, by Hory Shankar Mukerjee, Oxford/2013
2. Managing Soft Skills for Personality Development by B.N.Gosh, Tata McGraw-Hill/ 2012
3. Personality Development & Soft Skills by Barun K Mitra, Oxford/2011
4. Murphy, Herta A., Hildebrandt, Herbert W., & Thomas, Jane P., (2008) "Effective Business Communication", Seventh Edition, Tata McGraw Hill, New Delhi
5. Locker, Kitty O., Kaczmarek, Stephen Kyo, (2007), "Business Communication – Building Critical Skills", Tata McGraw Hill, New Delhi
6. Lesikar, Raymond V., &Flatley, Marie E., (2005)"Basic Business Communication – Skills for Empowering the Internet Generation", Tenth Edition, Tata McGraw Hill, New Delhi
7. Raman M., & Singh, P., (2006) "Business Communication", Oxford University Press, New Delhi.

Journals / Magazines:

1. Journal of Business Communication, Sage publications
2. Management Education, Mumbai

Websites:

www.mindtools.com
www.bcr.com

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Embedded Real Time Operating Systems

Course Code : **PI18PC210EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Justify the need of Real Time Operating System for Embedded Product. 2. Discuss RTOS scheduling policies to meet the deadlines along with different inter-process communication resources. 3. Analyze Linux kernel architecture with process & thread related APIs. 4. Categorize device drivers in Linux with corresponding shell commands. 5. Develop system integration with RTOS & acquire debugging techniques.	**At the end of the course, students will be able to:** 1. Differentiate OS, RTOS and classify Real-Time kernels. 2. Demonstrate the use of different scheduling algorithms to estimate the deadline and propose different inter-task-communication models opted in RTOS. 3. Describe Linux kernel architecture and process management. 4. Differentiate Linux user space processes and kernel space threads; and, implement device drivers using Shell APIs. 5. Suggest debugging methods to be opted for RTOS based designs.

UNIT – I

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS; Architecture of RTOS, Kernels – classifications, importance of scheduler in OS: objectives and functions; Hard versus Soft Real-time systems – examples, Jobs & Processes, timing constraints. Pre-emptive Vs Non pre-emptive kernels

UNIT – II

Task Priorities, Scheduling, Inter task Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section: Re-entrant Functions, Inter Process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.
Scheduling Algorithms – RMS, Preemptive EDF scheduling – principle, comparisons.

UNIT – III

Linux Kernel 2.x architecture – File system, Concepts of Process – creation, Process Control Block (PCB); process Vs thread; Concurrent Execution. Process Management in Linux – forks Vs Vfork; process state transitions, zombie state, Memory Management Algorithms.

UNIT – IV

Device Drivers – Definition; advantages of Modules; kernel space Vs user space; Concurrency and Race Conditions; classification of device drivers – character drivers, block drivers and net drivers; shell commands for drivers; IOCTLS and Tasklets

UNIT – V

Communicating with Hardware; Interrupt Handling. Debugging Techniques. Comparison of Linux 2.4 Vs 2.6 & 3.x with RT Linux concepts and porting on hardware. Case study of RTOS-RT Linux porting on LPC2148.

Suggested Reading:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-to-Use Modules in C", CMP Publishers Jan 1999.
2. Robert Love, "Linux Kernel Development" (3rd Edition), Novell Press 2010.
3. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
4. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, "Linux Device Drivers", 3rd Edition,O'Reilly Media Publishers
5. Real Time Systems, C.M.Krishna and G.Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Mixed Signal IC Design

Course Code : **PI18PC220EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Student should clearly distinguish between the features of mixed signal circuits and other circuits. 2. Students would be taught how to arrive at a given mixed signal circuit starting from the specifications 3. Students should be exposed to application areas during the lectures.	**At the end of the course, students will be able to:** 1. This course would generate a class of analog / mixed signal circuit designers 2. They would be able to address problems faced in the realization of systems using mixed signal circuits. 3. Produces a class of students who would be able to analyze a situation in the area of mixed signal circuits like switched capacitor circuits, data converters etc, starting from fundamentals.

UNIT – I

Introduction: concepts involved in mixed signal circuits – Analog & digital operations by the same circuit – Digital and analog circuits on the same substrate – Problems of covering both the types of circuits on the same substrate processes involved in a circuit which has analog / digital signals at the input and digital / analog of the output – mimicking analog components by digital operations (switched capacitor circuits).

Mixed signal functions – comparators sampling and sample and hold operations – Analog to Digital conversion and Digital / Analog conversion – phase and delay locked loops.

UNIT – II

Switched Capacitor Circuits (SCR) – switched capacitor resistor analysis of current and voltage waveforms – S.C.RS in series and parallel – Power dissipation in SCRFET switches charge in injection and clock feed though effects – limitations o f SCRs. Applications of SCR for (i) filters (ii) amplifiers / buffers, Integrators, Voltage multipliers, peak detectors, modulators etc.

Comparators: Basic architecture of a comparator specifications of a comparator op amp based comparator – limitations – modified comparators for improving performance Latched comparators for high speed applications Bi-polar comparators – BiCMOS comparators.

UNIT – III

Sample and hold circuits **–** specifications MOS sample and hold circuits – clock feed through and charge injection problems **–** S/H circuits with transmission gates – high input impedance S/H circuit – S/H circuits with improved slewing – Diode bridge based S/H circuits advantages and disadvantages of bridge based S/H circuits.

Data converters: Data converter fundamentals performance characteristics – Quantization noise.

UNIT – IV

Data converters, architecture: ideal A/D and D/A converters – Nyquist rate and over sampled D/A converters, philosophy and architectures of Nyquist rate D/A and A/D converters – philosophy and architectures of over sampled converters

Nyquist rate D/A converters: Decoder based converters, binary scaled converters, thermometric code converters, hybrid converters. Nyquist rate A/D converter: Integrating converters, successive approximation converters, Flash or parallel converters two step A/D converter, Cyclic A/D converter, pipe lined A/D converter – VCO based A/D converter.

UNIT – V

Architectures of over sampled A/D converter – 1 bit A/D and D/A converters Σ - Δ modulator, noise shaping and noise shaped A/D converter idle tones and dithering – system level description of over sampled A/D and D/A converters

Phase locked loop: What is phase locked loop and its importance in communication and instrumentation electronics – Basic architecture of a PLL - Analog PLL – Digital PLL – Locking limitations – Dynamics of PLL – lock range – Capture range – phase – frequency locked loop- charge pump based PLL – components of PLLs, frequency locked loop – Delay locked loop – applications of PLLs.

Suggested reading:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Physics of Semiconductor Devices

Course Code : **PI18PC230EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. To familiarize you with the modeling and the physical concepts behind the operation of microelectronic devices and enhance your appreciation for the field of high speed semiconductor devices and Non volatile memories used in VLSI systems.	**At the end of the course, students will be able to:** 1. Specify properties of semiconductors for construction of microwave components. 2. Identify and analyze microwave component performance using equivalent circuit analysis. 3. Employ JFET, MESFETs in different Microwave applications. 4. Analyse short channel effects in Semi Conductor Devices. 5. Describe the function of floating gate devices, transferred election devices and Microwave oscillators.

UNIT – I

Properties of Semiconductors: Crystal Structure Energy Bands, Carrier Transport Phenomena. (Mobility of Carriers, Resistivity and Hall Effect, Generation – Recombination Processes). High Field Phenomena. Gunn Effect and Negative Resistance Characteristics. Equation for Current Flow.

UNIT – II

Bipolar Devices: Ideal P-N Junctions, V-I Characteristics, Effect of Generation – Recombination Processes. Effect of High Injection. Junction Breakdown, Depletion and Diffusion Capacitance. Hetero Junctions. Bipolar Transistor – Characteristics – Equivalent Circuit – Ebers – Moll Model – Gummel Poon Model, Microwave and High Frequency Transistor Structures – Breakdown of Transistors including Secondary Breakdown.

UNIT – III

Field Effect Transistors – JFET, MESFET – Characteristics.
MOSFET and MISFET: MOS Diode – Capacitance Vs Voltage Curves. Interface Trapped Charges – oxide Charge. V-I Characteristics of MIS Diodes with Thin Insulating Films. MOS/MISFET – Different Types – Basic device Characteristics – Sub-threshold Region Characteristics – Buried Channel Devices.

UNIT – IV

Short Channel Effects – On sub-threshold Current, On Threshold Voltage – On the Structures – Shallow Junctions – Breakdown Voltage – Band Gap Engineering – Thin Film Transistor – Silicon On Insulator (SOI) Devices.

UNIT – V

Floating Gate Devices for Non-volatile Memories. MIOS Devices – Gallium Arsenide Devices – Gunn Devices (or Transferred Electron Devices TEDS) – Functional Devices for Microwave Oscillators. LEDS and Laser Diodes.

Suggested Reading:

1. S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, 1981.
2. Dewitt G. ONG., Modern MOS Technology: Processes, Devices and Design,Mc. Graw Hill Book Company. 1984.
3. CHEN , VLSI Hand book, CRC Press, IEEE Press, 2000.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Low Power VLSI Design

Course Code : **PI18PE210EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels 2. Apply leakage control mechanisms to reduce static power consumption in DSM VLSI regime 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Study and apply various software power estimation and optimization techniques for low power VLSI system design 5. Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs	**At the end of the course, students will be able to:** 1. Distinguish the impact of various power reduction techniques at different levels of VLSI Design 2. Identify the sources of power dissipation and apply leakage control techniques to reduce static power consumption in CMOS circuits 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Analyze different power reduction techniques for VLSI systems at Design time, Run-time and Stand-by modes 5. Employ software power estimation and optimization methods for low power VLSI system design 6. Apply low power circuit and architectural techniques such as capacitance reduction, gated clocking, VDD and Vth scaling, DVS etc in digital systems and SRAM designs

UNIT – I

Introduction to Low Power design: Why worry about power – at global and SOC levels, Emerging zero-power applications (WSN), 20 nm scenario, Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels)

Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design – Standby leakage control using transistor stacks, Multiple V_{TH} and dynamic V_{TH} techniques, Supply voltage scaling technique (Ref-1)

UNIT – II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories (Ref-2)

UNIT – III

Power Optimization Techniques – II: Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues (Ref-2) Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power (Ref-3)

UNIT IV

Low Voltage Low Power Static Random Access memories**:** Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, Loadless CMOS 4T SRAM cell, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction (Ref-1)

UNIT V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, Varying the clock speed, varying the V_{DD} of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

Contents beyond Syllabus:

Low Power Design for safety Critical applications: safe operation constraints vs low-power techniques, Unsuitable low power design techniques for safety critical applications, Low-power and safe-operating circuits. (4 hours)

Suggested Reading:

1. Kiat-Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata McGrawhill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, " Low-Power CMOS VLSI Circuit Design" , Wiley Pub., 2000 (Unit III)
4. Dimitrios Soudris, Christian Piguet and Coastas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002 (Topics beyond Syllabus)
5. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010 (for seminars and assignments)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Principles of VLSI System Design

Course Code : **PI18PE220EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Impart knowledge about VLSI design abstractions and hierarchies. Also impart knowledge on technology implications in VLSI design. 2. Impart knowledge about different circuit parameters that influences the performance of Static and dynamic CMOS circuits. 3. Impart knowledge about structured design strategies and different design approaches such as gate arrays standard cells and full custom design. 4. Impart knowledge about sub system design including different approaches for optimizing the performance. 5. Go through two case studies which illustrate the above mentioned methodologies leading to better understanding.	**At the end of the course, students will be able to:** 1. Acquainted about VLSI Design hierarchy and abstraction 2. Evaluate the performance of Static and dynamic CMOS circuits through estimation of associated circuit parameters like resistance capacitance etc. 3. Select different approaches for design of these circuits. 4. Apply structured approaches for designing VLSI subsystem and subsystems such as adders multipliers etc. 5. Study the system design approaches based on the two case studies illustrating how these methodologies are applied.

UNIT – I

Introduction to VLSI System design hierarchical design – design abstraction – different levels of abstraction and domains. Computer aided design VLSI design flow– technology implications and economics, issues connected with technology defect densities yield and die size, components of chips cost.

UNIT – II

Static and dynamic CMOS circuits, circuit characterizations and performance estimation: Resistance, Capacitance and Inductance – delay estimations power dissipation static and dynamic, design margining – reliability issues.

UNIT – III

CMOS design methods: Structured design strategies – Hierarchy, regularity modularity, chip design options: Programmable logic, logic structures: gate arrays, sea – of gate and gate array and standard cell based designs- standard cell libraries including I/O and ESD protection structures, design re- use and full custom mask design.

UNIT – IV

CMOs sub system design: Adders and Subtractors fast adders like carry by pass carry select and carry look ahead adders Multipliers, array and fast multipliers – Parity Generators - Zero-One Detectors – Binary Counters – Multiplexers – shifters – memory elements

UNIT – V

CMOs System case study: Core of RISC Micro Controller ALU address architectures, Instruction sets pipelining major blocks of the processor and 6 Bit Flash A/D Converter – high speed comparators and thermometer code converter.

Suggested Reading:

1. Weste Kamran Eshraghian, Principles of CMOS VLSI design – a Systems Perspective by NEILHE, Pearson Education Series, Asia, 2002.
2. Wolf, Modern VLSI Design, Pearson Education Series, 2002.
3. Jean M. Rabey, " Digital Integrated Circuits", Prentice Hall India, 2003

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Low Power Embedded Systems Design

Course Code : **PI18PE230EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT – I
Setting-up the software – tool chain. Setting-up the hardware – microcontroller master clock, basic Input/Output (I/O) techniques.

UNIT – II
Basic serial communication, serial communications using interrupts, analogue to digital conversion (ADC).

UNIT – III
Creating precise timing using timers. Interfacing to a liquid crystal display (LCD).

UNIT – IV
Accurately measuring time interval between input events – interrupts generated from input transitions and use of timers. Processor low power and sleep modes.

UNIT – V
Case studies for two applications followed by a mini project.

Suggested Reading:

1. Esin Terzioglu, et al, "Low Power Embedded Memory Design - Process to System Level Considerations".
2. Jong Wook Kwak; Ju Hee Choi; " Selective Access to Filter Cache for Low-Power Embedded Systems" 43rd Hawaii International Conference on System Sciences (HICSS).
3. A. Asaduzzaman, F.N.Sibai "Investigating Cache Parameters and Locking in Predictable and Low Power Embedded Systems", 22nd International Conference on Microelectronics.
4. T.S. Rajesh Kumar, C.P. Ravikumar, R. Govindarajan "Memory Architecture Exploration Framework for Cache Based Embedded SoC", 21st International Conference on VLSI Design.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

CPLD & FPGA Architectures and Applications

Course Code : **PI18PE240EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Implement given task using FPGA 2. Develop test pattern to test the FPGA 3. Design a product level approach utilizing FPGAs.	**At the end of the course, students will be able to:** 1. Differentiate between ROM,PAL,PLA,SPLD,CPLD,FPGA. 2. Compare the features of Various CPLDs interms of their architecture, Logic blocks. 3. Compare the features of Various FPGAs interms of their Architecture, Configurable logic block and routing. 5. Gain knowledge on routing algorithms adopted in FPGAs. 4. 5. Test a particular PLD using various techniques like design validation, Timing verification.

UNIT – I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT – II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT – III

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT – IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT – V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps.
Verification: introduction, logic simulation, design validation, timing verification.
Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Suggested Reading:

1. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Pearson Education 2009.
2. S. Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S. Brown, R. Francis, J. Rose, Z.Vransic, Field Programmable Gate array, Kluwer Publn, 1992.
5. Manuals from Xilinx, Altera, AMD, Actel.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

MEMS

Course Code : **PI18PE250EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Outcomes
At the end of the course, students will be able to:
1. A new and upcoming interdisciplinary area.
2. Generating better electronic gadgets
3. Technologies involving miniaturized electrical. Mechanical & electromechanical devices.
4. A new stream of electronics – MEMTRONICS (MEM based electronics)

UNIT – I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT – II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Deflection, Description of the above wrt. Fixed Beams. Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT – III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications

UNIT – IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT – V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

Suggested Reading:

1. Gabriel.M. Reviez, R.F. MEMS Theory, Design and Technology, Thon Wiley & Sons, 2003.
2. Thimo Shenko, Strength of Materials, CBS Publishers & Distributors.
3. K. Pitt, M.R. Haskard, Thick Film Technology and Applications, 1997.
4. Wise K.D. (Guest Editor), "Special Issue of Proceedings of IEEE", Vol.86, No.8, Aug 1998.
   Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

RFIC Design

Course Code : **PI18PE260EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Outcomes
At the end of the course, students will be able to:
1. Understand the design bottlenecks specific to RF IC design, linearity related issues, ISI
2. Identify noise sources, develop noise models for the devices and systems
3. Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
4. Comprehend different multiple access techniques, wireless standards and various transceiver architectures
5. Design various constituents' blocks of RF receiver front end

UNIT – I

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT – II

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT – III

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT – IV

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT – V

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

Suggested Reading:

1. BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.
3. B. Leunge, VLSI for Wireless Communication, Personal Education Electronics and VLSI series, Pearson Education, 2002.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Design and Simulation Laboratory - II

Course Code : **PI18PC211EC**	Instruction : 3 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1.5

Course Objectives	Course Outcomes
1. To Design analog and digital circuits with CMOS using EDA tools.	**At the end of the course, students will be able to:** 1. Familiarize the front end and back end tools to design Integrated Circuits. 2. Simulate the VTC of inverter under temperature and process variations. 3. Design and simulate the logic gates for given specifications. 4. Design and simulate the basic building blocks of analog integrated circuits. 5. Draw the layout and perform pre and post level simulations.

- Cadence Tool Introduction (Virtuoso schematic composer, spectre simulator).
- Simulate the characteristics of NMOS, PMOS transistor.
- Design and simulate the Symmetrical CMOS inverter.
- Design and Simulate the Voltage transfer characteristics of pseudo NMOS inverter.
- Design the two input NAND, NOR, AND, OR gates by considering Symmetrical CMOS inverter as a reference element and determine the propagation delay of the logic gates.
- Design the two input XOR, XNOR gates and determine the propagation delay of the logic gates.
- Design and simulation of Full adder and Full subtractor.
- Design and simulation of D Flip –Flop using transmission gates.
- Design and simulation of 4 bit adder
- Design and simulate basic current mirror for given Iref and determine VDSmin, Iout and Rout.
- Design a cascode current mirror for given Iref and determine VDSmin, Iout and Rout.
- Design of a CS amplifier (With different loads) for given specifications.
- Design a differential amplifier with active load (For PMOS input).
- Design a differential amplifier with active load (For NMOS input).
- Draw the layout for a logic gate and do the DRC,LVS, parasitic extraction and post simulation

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Embedded Systems Application Laboratory

Course Code : **PI18PC212EC**	Instruction : 3 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1.5

Course Objectives	Course Outcomes
1. Acquire skills to handle ARM powered cross compilers such as Embedded Studio IDE or Keil v5 µVision IDE in x86 Windows 7 & above or Linux 2.6 (Ubuntu 16.04 LTS) & above host. 2. Deploy an RTOS application in ARM CortexM4 board and run scheduling of multiple tasks. 3. Validate different RTOS scheduling algorithms in embOS RTOS for K66 MCU. 4. Use & Apply Inter Task Communication schemes to do preemptive multi-tasking. 5. Adopt debugging principles in embOS RTOS for ARM powered targets.	**At the end of the course, students will be able to:** 1. Demonstrate host to ARM target communication in embOS RTOS environment. 2. Configure emPower board with embOS and validate different scheduling algorithms. 3. Demonstrate different IPC schemes for multi-tasking in embOS with timing analysis. 4. Debug embedded application in RTOS with Cortex M4F ARM target at register-level. 5. Design to customize RTOS application with ARM MCU in the form of a mini project.

List of Experiments in RTOS using Embedded – C/C++:

Part – A
Real World Interfacing

1. Linux / embOS Real Time Task Creation Demonstration of Multi taksing.
2. Cooperative Scheduling Algorithm (Or) Round Robin Archiecture in RTOS.
3. Preemptive Scheduling Algorithm in embOS.
4. Resource Semaphore (Binary Semaphore) Demonstration.
5. Couting Semaphore IPC among the Linux / embOS tasks.
6. Message Queues & Mailboxes in Linux / embOS tasks.

Part – B
Mini Project

7. Mini project with the actual realization in the hardware powered with any standard MCUs available and prototying the application hardware.

(Or)

8. Study and implementation of Linux / embOS RTOS among the hardware peripharals available and prototyping a hard real time system design with emPower target.

Suggested tools for use :

1. Hardware Target CPU – Cortex M4F powered Segger Board
2. Embedded Software Development – Embedded Studio v 3.12a
3. Embedded Debugger – Cortex M4F ARM J Link
4. Hardware platform – Segger emPower board
5. RTOS – Linux / embOS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Mini Project

Course Code : **PI18PW219EC**	Instruction : 2 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1

Course Outcomes
At the end of the course, students will be able to:
1. Understand of contemporary / emerging technology for various processes and systems.
2. Share knowledge effectively in oral and written form and formulate documents.

The introduction of mini projects ensures preparedness of students to undertake major projects/dissertation. The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – II SEMESTER

Seminar – II

Course Code : **PI18PC218EC**	Instruction : 2 Hrs/week	CIE – Marks : 50
SEE – Marks : -	SEE - Duration : 3 Hours	Credits: 1

Course Objectives	Course Outcomes
1. Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	**At the end of the course, students will be able to:** 1. Selection of a suitable topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of project seminar report.

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Communication Engineering and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

DEPARTMENTOF ELECTRONICS AND COMMUNICATIONS ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION FOR
M.E (ECE) EMBEDDED SYSTEMS AND VLSI DESIGN
III and IV -SEMESTERS w.e.f. 2018-19 under CBCS

S. No	Category	Course code	Course Title	Scheme of Instruction			Scheme of Examination			Total	Credits
				L	T	P	Duration in Hrs	CIE	SEE		
III – SEMESTER											
1.	OE	PI18OE3XXXX	Open Elective	3	-	-	3	40	60	100	3
2.	PE	PI18PE3X0EC	Professional Elective - VI	3	-	-	3	40	60	100	3
3.	PW	PI18PW319EC	Dissertation-Phase-I / Internship	-	-	8	-	100	-	100	4
			Total	**6**	**-**	**8**	**-**	**180**	**120**	**300**	**10**
IV - SEMESTER											
1.	PW	PI18PW419EC	Dissertation-Phase-II / Internship	-	-	24	-	Viva-Voce (Grade)			**12**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Business Analytics

Course Code : **PI18OE310XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

Course Objectives	Course Outcomes
1. Understand the role of business analytics within an organization. 2. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization. 3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making. 4. To become familiar with processes needed to develop, report, and analyze business data. 5. Use decision-making tools/Operations research techniques. 6. Mange business process using analytical and management tools. 7. Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.	**At the end of the course, students will be able to:** 1. Students will demonstrate knowledge of data analytics. 2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics. 3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making. 4. Students will demonstrate the ability to translate data into clear, actionable insights

UNIT -I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT - II

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT – III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization

UNIT – IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT – V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

UNIT – VI

Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Suggested Reading:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Industrial Safety

Course Code : **PI18OE320XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

UNIT – I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT-II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment. Model Curriculum of Engineering & Technology PG Courses [Volume -II] 295

UNIT-III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-IV

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT-V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Suggested Reading:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Operations Research

Course Code : **PI18OE330XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

Course Outcomes
At the end of the course, students will be able to:
1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming
3. Students should able to carry out sensitivity analysis
4. Student should able to model the real world problem and simulate it.

UNIT - I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT - II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT - III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT - IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT - V

Competitive Models,Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Suggested Reading:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
5. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
6. Pannerselvam, Operations Research: Prentice Hall of India 2010
7. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Cost Management of Engineering Projects

Course Code : **PI18OE340XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

Introduction and Overview of the Strategic Cost Management Process Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Suggested Reading:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Composite Materials

Course Code : **PI18OE350XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

UNIT–I

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

Suggested Reading:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Waste to Energy

Course Code : **PI18OE360XX**	Instruction : 2 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: -

UNIT-I
Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II
Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT – III
Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for Model Curriculum of Engineering & Technology PG Courses [Volume -II] 299 thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT - IV
Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT – V
Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Suggested Reading:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Design for Testability

Course Code : **PI18PE310EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Outcomes
At the end of the course, students will be able to:
1. Modeling and simulation of digital circuits including various levels of modeling and different approaches for simulation. .
2. Different types of faults that occur in digital ICs. Concepts of detect ability of faults and fault coverage. Simulation of digital circuits with the presence of faults and evaluation of given test set for fault coverage.
3. Generate of test patterns for detecting single stuck faults in combinational and sequential circuits.
4. Concepts of controllability and observability and schemes for introducing testability into digital circuits which will make circuits more testable with ease and improve fault coverage.
5. Importance of built in self test (BIST) and different approaches for introducing BIST into logic circuits memories and embedded cores.

UNIT – I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT – II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT – III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT – IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Suggested Reading:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch., Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Integrated Optics & Photonic Systems

Course Code : **PI18PE320EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

Course Objectives	Course Outcomes
1. Understand the principles of integrated photonic circuits 2. Realise the various features and functions and types of photonic integrated circuits 3. Understand the active devices, passive devices, interconnects required to realize the integrated optical circuit 4. Understand the sources, receivers, amplifiers, system applications and advanced topics like microwave photonics and tera hertz devices 5. Study the fabrication methods of actives, passives, and interconnects	**At the end of the course, students will be able to:** 1. Apply the principles of optical waveguide theory to design passive optical components like waveguides 2. List various materials for photonic integrated circuits like semiconductors, polymers etc. 3. Compute the losses and performance metrics for integrated optics 4. Implement system models for integrated circuits 5. Apply the learned techniques for different applications

UNIT - I

Introduction, advantages, comparison of optical IC with electrical IC, applications of integrated optics, substrate materials for optical IC. Optical wave guide mode, modes in a planar wave guide, ray optic approach to optical mode theory, basic three layer waveguide, symmetric and asymmetric wave guide, rectangular channel and strip loaded wave guides. Wave guide fabrication technique, deposited thin film, substitution dopant atoms, carrier concentration reduction wave guide, epitaxial growth, electro optic wave guide.

UNIT - II

Polymer and fiber integrated optics, polymer processing, applications, polymer wave guide devices, optical fiber wave guide devices, fiber sensor, types, applications. Losses in optical wave guide, measurement of losses. Wave guide input and output couplers, types of couplers, coupling between wave guides, coupled mode theory, wave guide modulator,

UNIT - III

Electro optic modulator, single and dual channel electro optic modulator acousto optic modulator. Integrated semiconductor laser, integrated semiconductor optical amplifier, monolithical integrated direct modulator, direct modulation of QD laser, integrated optical detectors, structures, factors affecting the performance, principle of micro optical devices.

UNIT – IV

Optical amplifiers, semiconductor laser amplifier, doped fiber amplifiers, Fiber Raman amplifier, fiber Brillouin amplifier, noise characteristics ,crosstalk, system applications. Direct detection light wave system, digital optical receiver, direct detection with optical amplifiers, performance.

UNIT - V

Coherent detection light wave system, system configurations, performance. Soliton light wave system,soliton wave propagation, soliton amplification, system design.

Suggested Reading:

1. Robert Hunsperger, Integrated optics :Theory and technology 6/e Springer, 2009
2. Keico Iizuka, Elements of photonics, John Wiley, 2002
3. Pappannareddy, Introduction to light wave systems,Artech House,1995
4. Lifante, Integrated Photonics: Fundamentals ,John Wiley 2003

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

High Level Synthesis

Course Code : **PI18PE330EC**	Instruction : 3 Hrs/week	CIE – Marks : 40
SEE – Marks : 60	SEE - Duration : 3 Hours	Credits: 3

UNIT – I

Introduction to C-based FPGA Design , Using Vivado HLS HLS UltraFast Design Methodology Managing Interfaces Design Optimization RTL Verification, Exporting the RTL Design

UNIT – II

Introduction to the Vivado HLS C Libraries, Arbitrary Precision Data Types Library, The HLS Stream Library, HLS Math Library, Vivado HLS Video Library, The HLS IP Libraries, HLS Linear Algebra Library.

UNIT – III

Coding Styles: Unsupported C Constructs, The C Test Bench Functions, Loops, Arrays, Data Types. C++ Classes and Templates, Using Assertions, SystemC Synthesis.

UNIT – IV

Command Reference, Graphical User Interface (GUI) Reference, Send Feedback, Interface Synthesis Reference, AXI4 Slave Lite C Driver Reference, Video Functions Reference.

UNIT – V

HLS Linear Algebra Library, C Arbitrary Precision Types, C++ Arbitrary Precision Types, C++ Arbitrary Precision Fixed Point Types, Comparison of SystemC and Vivado HLS Types.

Suggested Reading:

1. Andres Takach, Creating C++ IP for High Performance Hardware Implementations of FFTs. DesignsDesignCon2002.
2. Preston A. Jackson, Cy P. Chan, Jonathan E. Scalera, Charles M. Rader, and M. Michael Vai - A Systolic FFT Architecture for Real Time FPGA Systems. MIT Lincoln Laboratory 244 Wood ST, Lexington, MA 02420
3. Vivado Design Suite User Guide and Vivado Design Suite Tutorial for High-Level Synthesis.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – III SEMESTER

Dissertation-Phase-I / Internship

Course Code : **PI18PW319EC**	Instruction : 8 Hrs/week	CIE – Marks : 100
SEE – Marks : -	SEE - Duration : -	Credits: 4

Course Objectives	Course Outcomes
1. Selection of a suitable for investigation for the project 2. Literature survey 3. Carrying out investigation / experiments including the selection of approaches to be adopted 4. Analysis of the results in interaction with the project guides. 5. Preparation of presentations and technical report.	**At the end of the course, students will be able to:** 1. Students go through the foundation needed for carrying out new investigations 2. Students would be ready with the problem to be investigated in phase II 3. They also get the training needed for presentations of their work.

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.
The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent /Very Good / Good/Satisfactory / Unsatisfactory

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SYLLABUS FOR M.E. (ECE-ES & VLSI) – IV SEMESTER

Dissertation-Phase-II / Internship

Course Code : **PI18PW419EC**	Instruction : 24 Hrs/week	CIE – Marks : **Viva-Voce Grade**
SEE – Marks :	SEE - Duration :	Credits: 12

Course Objectives	Course Outcomes
1. Carrying out further literature survey related to the topic already selected. 2. Carrying out investigation experiments, simulation in relation to the problem. 3. Problem analysis and solution finding for problems encountered 4. Organization of results 5. Thesis preparation, presentation and defence.	**At the end of the course, students will be able to:** 1. Students will be able to face any new problem and find a sensible solution 2. Students would be trained to investigate a given problem in a systematic way 3. They would be ready to take up work which may be needed by the industry.

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.
The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent /Very Good / Good/Satisfactory / Unsatisfactory