VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, IBRAHIMBAGH, HYDERABAD-31

M.E./M.Tech. (CBCS) I-Semester Make up Examinations, March-2017

No. 705/M.E./M.Tech./Exams/TT/2017

TIME TABLE

Date: 06-03-2017

Timings: 10.00 am to 1.00 pm

DATE / DAY	E.C.E.		E.E.E.	MECHANICAL	C.S.E.
	Communication Engineering & Signal Processing	**Embedded Systems & VLSI Design**	**Power Systems & Power Electronics**	**Advanced Design & Manufacturing**	
14-03-2017 Tuesday	Microcontrollers and DSP Processors - Architecture	Embedded Systems Design	---	Mathematical Methods for Engineers	Mobile Computing
16-03-2017 Thursday	Advance Digital Signal Processing	Digital IC Design	Power System Stability	Metal Cutting and Forming	Information Storage & Management
18-03-2017 Saturday	Advance Digital Modulation Techniques	Analog IC Design	Power Electronic Converters	---	Advanced Algorithms
20-03-2017 Monday	---	Physics of Semiconductor Devices	High Voltage DC Transmission	Finite Element Techniques	---
22-03-2017 Wednesday	Adaptive Signal Processing	Advanced Computer Organization	Renewable Energy Sources	Theory of Elasticity and Plasticity	Artificial Intelligence
24-03-2017 Friday	---	VLSI Technology	Power Quality Engineering	---	Object Oriented Software Engineering
27-03-2017 Monday	---	---	---	---	Finishing School-I (10.00 am to 11.30 am)

Sd/-
Controller of Examinations

Copy to:

1. The Principal, VCE for information.
2. The Director, Academic and Administration, VCE.
3. The Director, Admissions and Examinations, VCE.
4. The Head, Department of CSE/ECE/EEE/Mech. Engg./H&SS/Mathematics, VCE.

} with a request to bring it to the notice of all concerned.

5. The Coordinator, Computer Centre, VCE, with a request to upload the timetable in the college website.