DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SYLLABUS FOR B.E. VI SEMESTER

INTRODUCTION TO VERILOG HDL

(for other Branches)

Instruction: 2 Hrs /week	SEE Marks : 70	Course Code : OE640EC
Credits : 2	CIE Marks : 30	Duration of SEE : 3 Hrs

Course Objective	Course Outcomes
1. To familiarize with various modeling styles: structural, dataflow and behavioral of Verilog HDL. 2. To develop combinational and sequential circuits using various modeling styles of Verilog HDL.	**At the end of the course, students will be able to:** 1. Students can model digital circuits using Verilog. 2. Implement and distinguish different Verilog HDL modeling styles. 3. Construct and analyze Verilog HDL models of combinational and sequential circuits. 4. Design and develop Verilog HDL modeling and test bench for digital systems for the given specifications.

UNIT - I

INTRODUCTION TO VERILOG: Verilog as HDL, Levels of Design Description, Basic Concepts of Verilog, Data Types, System Tasks, Compiler Directives, Modules and Ports.

GATE LEVEL MODELING: Introduction, Primitive Gate types, Gate Delays, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Digital Circuits with Gate Primitives, Delays.

UNIT - II

DATA FLOW LEVEL MODELING: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators, Design Examples.

SWITCH LEVEL MODELING: Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives and Delays, Design Examples.

UNIT - III

BEHAVIORAL MODELING: Introduction, Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, multi-way branching, Loops, Sequential and Parallel blocks, Generate blocks, Design Examples.

UNIT - IV

FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES: Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines).

Suggested Reading:

1. Samir Palnitkar, —Verilog HDL A Guide to Digital Design and Synthesis,‖ 2nd Edition, Pearson Education, 2006.
2. Michael D. Ciletti, " Advanced Digital Design with Verilog HDL", PHI, 2005.
3. J. Bhasker, —A Verilog HDL Primer,‖ 2nd Edition, BS Publications, 2001.