VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, IBRAHIMBAGH, HYDERABAD-31

M.E./M.Tech. (CBCS) II-Semester Make up Examinations, September-2017

No.895/M.E./M.Tech./Exams/TT/2017

TIME TABLE

Date: 23-08-2017

Timings: 10.00 am to 1.00 pm

DATE / DAY	E.C.E.		E.E.E.	MECH. ENGG.	C.S.E.
	Communication Engineering & Signal Processing	**Embedded Systems & VLSI Design**	**Power Systems & Power Electronics**	**Advanced Design & Manufacturing**	
06-09-2017 Wednesday	Coding Theory and Techniques	Mixed Signal IC Design	Distribution System Planning and Automation	Design for Manufacture and Assembly	---
08-09-2017 Friday	---	Embedded Real Time Operating Systems	---	Metallurgy of Metal Casting and Welding Processes	---
11-09-2017 Monday	Wireless Communications and Networking	Low Power VLSI Design	Machine Modeling and Analysis	Computer Aided Mechanical Design and Analysis	Image Processing
13-09-2017 Wednesday	---	Design for Testability	---	Mechanical Vibrations	---
15-09-2017 Friday	Image and Video Processing	VLSI Physical Design	Modern Control Theory	Additive Manufacturing	Cloud Computing -
18-09-2017 Monday	---	CPLD & FPGA Architectures and Applications	Programmable Logic Controllers and their Applications	Experimental Techniques and Data Analysis	---
21-09-2017 Thursday	Finishing School-II (10.00 am to 11.30 am)	Finishing School-II (10.00 am to 11.30 am)	Finishing School-II (10.00 am to 11.30 am)	Finishing School-II (10.00 am to 11.30 am)	Finishing School-II (10.00 am to 11.30 am)

Sd/-
Controller of Examinations

Copy to:

1. The Principal, VCE for information.
2. The Director, Admissions and Examinations, VCE.
3. The Head, Department of CSE/ECE/EEE/Mech. Engg./H&SS/Mathematics, VCE

} with a request to bring it to the notice of all concerned.

4. The Coordinator, Computer Center, VCE, with a request to upload the timetable in the college website.
5. The Librarian, VCE, for information.