DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Scheme of Instruction
and
Syllabi of

M.E. (ECE)
EMBEDDED SYSTEMS
AND
VLSI DESIGN
(With effect from 2014-2015)

VASAVI COLLEGE OF ENGINEERING
(Autonomous Institution Under UGC)
Ibrahimbagh, Hyderabad - 500 031
Andhra Pradesh
### Scheme of Instruction & Examination

**M.E. – Four Semester Course (Regular)**

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject</th>
<th>Periods per week</th>
<th>Duration (Hours)</th>
<th>Max. Marks</th>
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**Semester – II**

|        |                          |                  |                  |            |         |         |
| 1.     | Core                     | 4                | --               | 3          | 70       | 30      | 3       |
| 2.     | Core                     | 4                | --               | 3          | 70       | 30      | 3       |
| 3.     | Core / Elective          | 4                | --               | 3          | 70       | 30      | 3       |
| 4.     | Core / Elective          | 4                | --               | 3          | 70       | 30      | 3       |
| 5.     | Core / Elective          | 4                | --               | 3          | 70       | 30      | 3       |
| 6.     | Elective                 | 4                | --               | 3          | 70       | 30      | 3       |
| 7.     | Lab – III                | --               | 3                | --         | 50       | 2       |
| 8.     | Lab – IV                 | --               | 3                | --         | 50       | 2       |
| 9.     | Seminar – II             | --               | 3                | --         | 50       | 2       |
|        |                          | **Total**        | 24               | 9          | **420**  | **330** | 24      |

**Semester – III**

|        |                          |                  |                  |            |         |         |
| 1.     | Dissertation + Project Seminar* | -- | -- | -- | -- | 100** | 6 |
|        |                          | **Total**        | --               | 6          | --       | 100**  | 6 |

**Semester – IV**

|        |                          |                  |                  |            |         |         |
| 1.     | Dissertation             | --               | --               | Viva-voce  | Grade*** | -      | 10      |
|        |                          | **Total**        | --               | --         | --       | --     | 10      |

Note: Six core Subjects and Six Elective subjects should be completed by the end of Semester – II.

* One Project Seminar presentation.

** 50 marks to be awarded by guide and 50 marks to be awarded by Viva committee with guide and two internal faculty members.

*** Excellent / Very Good / Good / Satisfactory / Unsatisfactory.

(i) The syllabus consists of 5 units. Semester end examination will be conducted for 70 marks. The question paper consists of PART - A and PART - B. Part - A is compulsory and should cover the entire syllabus, and carries 20 marks. Part - B will comprise seven questions. There has to be one question in each unit of the syllabus and the remaining two questions may be from the entire syllabus of all 5 units. Student has to answer any five questions out of seven questions and each question carry 10 marks. Theory question paper have total 8 questions out of which candidate has to answer 6 questions including one compulsory question of 20 marks. This compulsory question, consisting of 10 questions, which will cover the entire syllabus. Other questions will be of 10 marks each.

(ii) Two internal examinations will be conducted for 20 marks. The question paper consists of Part - A and Part - B. Student should answer all the questions from Part - A and any two questions from Part - B. Part - A carries 6 marks and it consists of 6 questions. Each question is awarded 1 marks. The question may be definition, problem solving, multiple choice, match the following and filling the blanks type. Part – B carries 14 marks and consists of 3 Questions. Each question carries 7 marks and it may contain 2 sub questions.
### List of Subjects for ME (ECE) Course with specialization in EMBEDDED SYSTEMS AND VLSI DESIGN

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<td>Graph Theory and Its Applications to VLSI</td>
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<td>System Design and Reliability</td>
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<td>Design of Fault Tolerant Systems</td>
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EC 5010
MICROCONTROLLERS FOR EMBEDDED SYSTEMS DESIGN

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UNIT – I

UNIT – II
C51 Architecture, Instruction Set, Addressing Modes, Timers and Counters, Serial Communication, Interrupt Programming in Embedded-C. Interfacing with External Memory, Expansion of I/O Ports with PPI (8255).

UNIT – III
C51 Real World Interfacing using Embedded C: ADC0804/08, DAC, LCD, Keypad, RTC, DC Motor, Stepper Motor and PWM programming.

UNIT – IV
Introduction to RISC concepts with ARM as CPU, ARM7 (LPC2148) engine Architecture, AMBA Bus, Registers, Programming Modes, Importance of Thumb Mode, CPSR, SPSR, Pipeline, Exceptions, Interrupts and vector table; Core Extensions, ARM Revisions, ARM processor families. ARM Programming Model.

UNIT – V
Embedded Software Development Tools: Host and Target Machines, cross compiler, assemblers, linkers, loaders and locators for Embedded Software Debugging Techniques: Testing on Host Machine, JTAG, Instruction Set Simulators, Logic Analyzers; Comparative Case Study on GSM based Embedded System design with C51 Vs ARM7.

Suggested Reading:

EC 5020  
DIGITAL IC DESIGN

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UNIT – I
Building blocks for digital design: multiplexer, demultiplexer, decoder, encoder, comparator, adders, building blocks with memory: clocked building blocks, register-building blocks, RAM, ROM, PLA, PAL.

UNIT – II
Hardware description languages: hierarchical modeling concepts, modules, module instances, design and stimulus blocks: gate level, data flow, behavioral modeling techniques (Verilog), switch level modeling, delays.

UNIT – III
Combinational circuits: design of CMOS logic circuits based on the Boolean expressions. Differential CMOS circuits. Static CMOS digital latches, static random-access memory cell, d-ram cell, dynamic CMOS latches.

UNIT – IV
Synchronous and asynchronous system design techniques and their minimization, Gray-code counter, BiCMOS logic gates. Pseudo-NMOS and dynamic pre-charging. Domino-CMOS logic, no race logic, single-phase dynamic logic, differential CMOS logic, dynamic differential logic.

UNIT – V
Top down design, Finite State Machine (FSM), case studies (traffic signal controller), synchronization failure and meta stability, Algorithmic State Machines (ASMS), synthesis and test benches- using Verilog.

Suggested Reading:

EC 5030

ANALOG IC DESIGN

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UNIT – I
Introduction: What are electronic devices and circuits - Types of electrical signals - Characteristics of analog signals - Analog functions - Devices characteristics needed to perform these functions. Discrete component approach to analog circuit - Integrated circuit approach, silicon as base material. Integrated circuit – Components for ICs - Resistors, Capacitors, inductors diodes, BJTS, MOSFETS - Their IC architectures, limitations, circuits design philosophies - Different families of circuits device models. Basic analog circuits - Amplifiers - Different type of loads - Biasing techniques - current mirrors - Coupling techniques between stages.

UNIT – II

UNIT – III

UNIT – IV
Operational amplifiers - characteristics and specifications - Two and three stage Op-Amps - analysis of gain, frequency and phase response - Coupling problems, fully differential amplifiers - Cacodes, folded cascades - common mode feedback, and circuits, active cascade Op-Amp - current differential amplifiers – current feedback Op-Amps, - Gilbert Cells. OTAS.

UNIT – V
Oscillators and mixers: Basics of oscillators - Feedback oscillators, negative resistance oscillators, (two port oscillators), ring oscillators - Differential ring oscillators, LC oscillators, relaxation oscillators, voltage controlled oscillators, Tuning delay and frequency.

Suggested reading:
WITH EFFECT FROM THE ACADEMIC YEAR 2014-2015

EC 5040

MIXED SIGNAL IC DESIGN

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UNIT – I
Introduction: concepts involved in mixed signal circuits - Analog & digital operations by the same circuit - Digital and analog circuits on the same substrate - Problems of covering both the types of circuits on the same substrate processes involved in a circuit which has analog / digital signals at the input and digital / analog of the output – mimicking analog components by digital operations (switched capacitor circuits).
Mixed signal functions - comparators sampling and sample and hold operations - Analog to Digital conversion and Digital / Analog conversion – phase and delay locked loops.

UNIT – II
Switched Capacitor Circuits (SCR) - switched capacitor resistor analysis of current and voltage waveforms - S.C.RS in series and parallel - Power dissipation in SCRFET switches charge in injection and clock feed though effects - limitations of SCRs. Applications of SCR for (i) filters (ii) amplifiers / buffers, Integrators, Voltage multipliers, peak detectors, modulators etc.
Comparators: Basic architecture of a comparator specifications of a comparator op amp based comparator - limitations - modified comparators for improving performance Latched comparators for high speed applications Bi-polar comparators - BiCMOS comparators.

UNIT – III
Sample and hold circuits - specifications MOS sample and hold circuits - clock feed through and charge injection problems - S/H circuits with transmission gates - high input impedance S/H circuit - S/H circuits with improved slewing - Diode bridge based S/H circuits advantages and disadvantages of bridge based S/H circuits.
Data converters: Data converter fundamentals performance characteristics - Quantization noise.

UNIT – IV
Data converters, architecture: ideal A/D and D/A converters - Nyquist rate and over sampled D/A converters, philosophy and architectures of Nyquist rate D/A and A/D converters - philosophy and architectures of over sampled converters

UNIT – V
Architectures of over sampled A/D converter - 1 bit A/D and D/A converters Σ - Δ modulator, noise shaping and noise shaped A/D converter idle tones and dithering - system level description of over sampled A/D and D/A converters
Phase locked loop: What is phase locked loop and its importance in communication and instrumentation electronics - Basic architecture of a PLL - Analog PLL - Digital PLL - Locking limitations - Dynamics of PLL - lock range - Capture range - phase - frequency locked loop- charge pump based PLL - components of PLLs, frequency locked loop - Delay locked loop - applications of PLLs.

Suggested reading:
EC 5050

EMBEDDED REAL TIME OPERATING SYSTEMS

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UNIT – I
Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS; Architecture of RTOS, Kernels – classifications, importance of scheduler in OS: objectives and functions; Hard versus Soft Real-time systems – examples, Jobs & Processes, timing constraints. Preemptive Vs Non preemptive kernels

UNIT – II
Task Priorities, Scheduling, Inter task Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section – Reentrant Functions, Inter Process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

UNIT – III
Brief Review of Unix Operating Systems; Linux Kernel 2.4 architecture – File system, Concepts of Process – creation, Process Control Block (PCB); process Vs thread; Concurrent Execution. Process Management in Linux – forks Vs Vfork; process state transitions, zombie state, Memory Management Algorithms, Shell programming. Comparison of Linux 2.6 kernel with 2.4

UNIT – IV
Device Drivers – Definition; advantages of Modules; kernel space Vs user space; Concurrency and Race Conditions; classification of device drivers - character drivers, block drivers and net drivers; shell commands for drivers; IOCTLS and Tasklets

UNIT – V
Communicating with Hardware; Interrupt Handling; Debugging Techniques;
Comparison of RTOS – VxWorks, µC/OS-II and RT Linux for Embedded Applications

Suggested Reading:
EC 5060

VLSI PHYSICAL DESIGN

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UNIT – I
Scope of physical design – Components of VLSI – Various layers of VLSI – Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

UNIT – II

UNIT – III
Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT – IV
Cell concepts – cell based layout design – Wein-berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnect delay modeling, floor planning, routing and clock distribution.

UNIT – V
CAD Tools: Layout editors, Design rule checkers, circuit extractors – Hierarchical circuit extractors – Automatic layout tools, silicon compilers, modeling and extraction of circuit parameters from physical layout.

Suggested Reading:
EC 5011

DESIGN AND SIMULATION LABORATORY-I

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Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Design and simulation of combinational circuits
(ii) Design and simulation of sequential circuits
(iii) Design and simulation of mixed signal circuits
(iv) Microcontroller programming
   a. Toggling the LEDs,
   b. serial data transmission,
   c. LCD and Key pad interface
EC 5012

EMBEDDED SYSTEMS LABORATORY

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List of Experiments using Embedded C/Embedded C++:

1. To toggle LEDs connected to GPIOs of AT89S52 with some intentional Delay.
2. To design & implement 4x3 matrix Keypad Device Driver for ASCII mapping.
3. To design & implement 2x16 LCD Device Driver for displaying below text:
   
   Line-1: "Welcome@ESD Lab!"
   Line-2: "Enter to Proceed"

4. To Configure Timer0 and Timer1 for intended delay without interrupts.
5. To design & demonstrate the UART drivers for data transmission and data reception at 9600bps full duplex baud.
6. To design & implement the concept of writing Interrupt Service Routine (ISR) for external interrupt INT0, INT1.
7. To design & implement the concept of mixing of external ISRs with Internal ISRs and understanding the ISR handling process.
8. To design & implement LED Seven Segment driver with adjustable delay.
9. To design & implement User Centric template Menu designs in Embedded C
10. To design & implement User Centric template Menu designs in Embedded C++.

Suggested tools for use:

1. Hardware Target CPU – AT89S52
2. Embedded Software Development – Keil μVision4 IDE
3. Embedded Debugger – Keil μVision4 Debugger
4. Hardware Simulator – Proteus

Note: The experiments will be decided and modified if necessary and conducted by the lecturer concerned.
EC 5013

DESIGN AND SIMULATION LABORATORY-II

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Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Synthesis of combinational circuits (4 to 6 MSI digital blocks).
(ii) Synthesis of sequential circuits (4 to 6 MSI digital blocks).
(iii) Schematic simulation, layout, DRC, LVS, parasitic extraction for cells (inverter, NAND gate, NOR gates).
(iv) Programming using real time operating systems
    a. Multi tasking using round robin scheduling
    b. IPC using message queues
    c. IPC using semaphore
    d. IPC using mail box
EC 5014

EMBEDDED SYSTEMS APPLICATIONS LABORATORY

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List of Experiments using Embedded – C/Embedded C++:

1. Stepper Motor Interfacing
2. DC motor interfacing
3. RTC Interfacing
4. Watchdog Programming
5. SRAM CY62256 32KBSRAM interfacing
6. ADC0804/ADC0808 interfacing
7. SAR DAC0804 interfacing
9. Porting RTX51 Full RTOS and scheduling of fast tasks, standard tasks & ISRs

Suggested tools for use:

1. Hardware Target CPU – AT89S52
2. Embedded Software Development – Keil µVision4 IDE
3. Embedded Debugger – Keil µVision4 Debugger
4. Hardware Simulator – Proteus
5. RTOS – RTX51 Tiny & RTX51 Full

Note: The experiments will be decided and modified if necessary and conducted by the lecturer concerned.
EC 5015

SEMINAR - I

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Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Communication Engineering and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.
EC 5016

SEMINAR - II

| Instruction     | 3 Periods per week | External Examination - Duration | -
|------------------|--------------------|----------------------------------|---
| Sessionals       | 50 Marks           | External Examination - Marks     | -
| Credits          | 02                 |                                  | ---

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Communication Engineering and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.
EC 5017

PROJECT SEMINAR

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The main objective of the Project Seminar is to prepare the students for the dissertation to be executed in 4th semester. Solving a real life problem should be focus of Post Graduate dissertation. Faculty members should prepare the project briefs (giving scope and reference) at the beginning of the 3rd semester, which should be made available to the students at the departmental library. The project may be classified as hardware / software / modeling / simulation. It may comprise any elements such as analysis, synthesis and design.

The department will appoint a project coordinator who will coordinate the following:
- Allotment of projects and project guides.
- Conduct project - seminars.

Each student must be directed to decide on the following aspects
- Title of the dissertation work.
- Organization.
- Internal / External guide.
- Collection of literature related to the dissertation work.

Each student must present a seminar based on the above aspects as per the following guidelines:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through OHP, PC followed by a 10 minutes discussion.
3. Submit a report on the seminar presented giving the list of references.

Project Seminars are to be scheduled from the 3rd week to the last week of the semester. The internal marks will be awarded based on preparation, presentation and participation.
EC 5018

DISSERTATION

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The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student’s presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carried out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent / Very Good / Good / Satisfactory / Unsatisfactory
EC 5070

LOW POWER VLSI DESIGN

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UNIT – I
Introduction and need of low power design, sources of power dissipation, MOS transistor leakage components, SOI technology, FinFET, Back gate FET, power and energy basics, power dissipation in CMOS circuits, Energy-delay product as a metric, design strategies for low power.

UNIT – II

UNIT – III

UNIT – IV

UNIT V
Introduction to bio-medical signals – ECG, EEG, EMG; Amplifiers for bio-signals, Frequency Ranges of Various bio-Signals, Leakage current reduction in medical devices, Signal conditioning and data acquisition.

Suggested Reading:
EC 5080

DESIGN FOR TESTABILITY

Instruction | 4 Periods per week | External Examination - Duration | 3 Hours
---|---|---|---
Sessionals | 30 Marks | External Examination - Marks | 70 Marks
Credits | 03

UNIT – I
Introduction to Test and Design for Testability (DFT) Fundamentals.
Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling.
Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT – II

UNIT – III
Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT – IV
Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V
Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Suggested Reading:

EC 5090

PHYSICS OF SEMICONDUCTOR DEVICES

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UNIT – I

UNIT – II

UNIT – III

UNIT – IV

UNIT – V

Suggested Reading:
EC 5100

PRINCIPLES OF VLSI SYSTEM DESIGN

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UNIT – I
Introduction to VLSI System design hierarchical design – design abstraction – different levels of abstraction and domains. Computer aided design VLSI design flow – technology implications and economics, issues connected with technology defect densities yield and die size, components of chips cost.

UNIT – II
Static and dynamic CMOS circuits, circuit characterizations and performance estimation: Resistance, Capacitance and Inductance – delay estimations power dissipation static and dynamic, design margining – reliability issues.

UNIT – III
CMOS design methods: Structured design strategies – Hierarchy, regularity modularity, chip design options: Programmable logic, logic structures: gate arrays, sea – of gate and gate array and standard cell based designs- standard cell libraries including I/O and ESD protection structures, design re-use and full custom mask design.

UNIT – IV
CMOs sub system design: Adders and Subtractors fast adders like carry by pass carry select and carry look ahead adders Multipliers, array and fast multipliers – Parity Generators - Zero-One Detectors – Binary Counters – Multiplexers – shifters – memory elements

UNIT – V
CMOs System case study: Core of RISC Micro Controller ALU address architectures, Instruction sets pipelining major blocks of the processor and 6 Bit Flash A/D Converter – high speed comparators and thermometer code converter.

Suggested Reading:
EC 5110
ADVANCED COMPUTER ORGANIZATION

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UNIT – I
Processor Design: CPU Organization, Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating Point Arithmetic, Instruction Pipelining, Super Scalar techniques, Linear pipeline processors, Super scalar and super pipeline design, Multi vector and SIMD computers.

UNIT – II
Control Unit Design: Basic Concepts: Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Micro program sequencer, Case studies based on both the approaches.

UNIT – III
Memory Organization: Internal memory, computer memory system overview, the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT – IV
I-O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Bus Arbitration; Synchronous bus and asynchronous bus, Interface circuits, Parallel port, Serial port, standard I/O interfaces, IO Processor, PCI bus, SCSI bus, USB bus protocols.

UNIT – V
Parallel Computer Systems: Instruction Level Parallelism (ILP) – Concept and Challenges, Dynamic Scheduling, Limitations on ILP, Thread Level Parallelism, Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors and Super computers.

Suggested Reading:

EC 5120

CPLD & FPGA ARCHITECTURES AND APPLICATIONS

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UNIT – I
Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT – II
FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA’s- XILINX XC4000, Virtex-II FPGA’s, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA’s, Actel FPGA’s, AMD FPGA.

UNIT – III
CPLD’s: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD’s, max 7000 series CPLD’s, AT & T – ORCA’s (Optimized Reconfigurable Cell Array), Cypress flash 370 device technology, lattice PLSI’s architectures.

UNIT – IV

UNIT – V
Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps. Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Suggested Reading:
5. Manuals from Xilinx, Altera, AMD, Actel.
EC 5130

VLSI TECHNOLOGY

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UNIT – I

UNIT – II

UNIT – III
Oxide Growth: Structure of SiO₂, Growth Mechanism and Dynamics – Oxide Growth by Thermal method.

UNIT – IV
Deposition techniques Chemical Vapour Deposition (CVD) and associated methods like LPCVD and PECVD. PVD thermal evaporation and sputtering. Step coverage issues.
Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their characteristics, optical exposure systems contact and projection systems, steppers, X-ray – Electron Beam Lithography.
Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT – V
Ion implantation: Range and Penetration Depth – Damage and Annealing – Ion Implantation machine.

Suggested Reading:
2. CY Chang and S.M. SZe , VLSI Technology, Tata Mc Graw-Hill Companies Inc.
EC 5140

MEMS

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UNIT – I
Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT – II

UNIT – III
Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications

UNIT – IV

UNIT – V

Suggested Reading:
EC 5150

SYSTEM ON CHIP ARCHITECTURE

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UNIT – I

UNIT – II

UNIT – III

UNIT – IV

UNIT – V
System in Package Design: Advantages and disadvantages between SoC, SiC and board level design; SiP Design flow, System Planning, Chip-Package co-design, System Optimization; SiP Design Layout, Simulation, Verification; Gaps in SiP Design, Power optimization tools, Parasitic extraction tools, Signal Integrity. Examples of SiP.

Suggested Reading:
3. Jason Andrews, Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), BK and CDROM.
EC 5160

SCRIPTING LANGUAGES FOR EMBEDDED SYSTEMS

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UNIT – I
Overview of scripting languages- PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT – II
Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT – III
Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions. Inter process communication,- signals, files, pipes, sockets,.

UNIT – IV
Threads- process model, thread model, Perl debugger- using debugger commands, customization, internals and externals, internal data types, extending Perl, embedding Perl, exercises for programming using Perl.

UNIT – V
Other languages: Broad features of other scripting languages SKILL, CGI, java script, VB script.

Suggested Reading:
EC 5170

VLSI SIGNAL PROCESSING

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UNIT – I

UNIT – II

UNIT – III

UNIT – IV

UNIT – V

Suggested Reading:
EC 5180  
**GRAPH THEORY & ITS APPLICATIONS TO VLSI**

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UNIT – I
Introduction: Basic definitions, results and examples relating to Graph theory, self-complementing graphs and properties of graphs, Trees, Spanning tree & directed graphs.

UNIT – II
Definitions of strongly, weakly, unilaterally connected graphs and deadlocks. Metric representation of graphs. Classes of graphs: standard results relating to characterization of Hamiltonian graphs, standard theorems

UNIT – III
Self-centered graphs and related theorems. Chromatic number vertex and edge – application to coloring, linear graphs, Euler’s formula.

UNIT – IV
Graph algorithms: DFS – BFS algorithms, min. spanning tree and max. spanning tree algorithm. Directed graphs algorithms for matching, properties flow in graph and algorithms for max flow. PERT-CPM, complexity of algorithms, P-NP – NPC – NP hard problems and examples.

UNIT – V

Suggested Reading:
EC 5190
SYSTEM DESIGN AND RELIABILITY

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UNIT – I
System design aspects- Structure of systems in general-hardware, software components, testability of systems, and design of systems from testability point of view.

UNIT – II
System Reliability: Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces. Test environments, testing for reliability and durability, failure reporting,

UNIT – III

UNIT – IV

UNIT – V
System level reliability testing, - Reliability evaluation and screening procedures at system level. Life tests for systems, accelerated testing reliability costs, Standards for system level reliability evaluation and screening.

Suggested Reading:
EC 5200

HARDWARE – SOFTWARE Co-DESIGN

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UNIT –I

UNIT –II
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Suggested Reading:
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
EC 5210  
ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

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UNIT – I
Introduction and Sources of EMI: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT – II
Types of Electromagnetic Coupling: Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near78 Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT – III
EMI Measurements: EMI Shielded Chamber, Open Area Test Site, TEM Cell, GTEM cell Sensors/ Injectors/ Couplers, LISN, voltage probe, Current probe Test beds for ESD and EFT.

UNIT – IV
EMI Mitigation Techniques: Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT – V

Suggested Reading:
EC 5220

DESIGN OF FAULT TOLERANT SYSTEMS

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UNIT – I
Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT – II
Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT – III
Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller’s expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT – IV
Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA’s, One’s counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT – V
Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

Suggested Reading:
1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI.
EC 5230

MICROWAVE INTEGRATED CIRCUITS

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<th>External Examination - Duration</th>
<th>3 Hours</th>
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UNIT – I

UNIT – II

UNIT – III

UNIT – IV
Lumped Elements for MIC’s Design and fabrication of lumped elements, circuits using lumped elements.

UNIT – V
Nonreciprocal components for MIC’s Microstrip on Ferrimagnetic substrates, Microstrip circulators. Isolators and phase shifters. Design of microstrip circuits – high power and low power circuits.

Suggested Reading:
2. Leo Young, Advances in Microwaves, Academic Press.
EC 5240

OPTIMIZATION TECHNIQUES

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UNIT – I
Use of optimization methods. Introduction to classical optimization techniques, motivation to the simplex method, simplex algorithm, sensitivity analysis.

UNIT – II

UNIT – III

UNIT – IV
Review of a global optimization techniques such as Monte Carlo method, Simulated annealing and Tunneling algorithm.

UNIT – V
Generic algorithm - Selection process, Crossover, Mutation, Schema theorem, comparison between binary and floating point implementation.

Suggested Reading: