VASAVI COLLEGE OF ENGINEERING (Autonomous)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 27.05.2024

Minutes of the 15th meeting of Board of Studies in Electronics and Communication Engineering held on 18.5.2024 (Saturday) at 10.30 a.m.

Members Present:

1.	Dr. E. Sreenivasa Rao Professor & Head	:	Chairman, BoS
2.	Dr. Rajendra Naik Professor, Osmania University, Hyderabad.	:	Osmania University Nominee & Member
3.	Dr. Sreehari Rao Patri Professor, Department of ECE, NIT-Warangal.	:	Member
4.	Sri. D.V.R. Murthy Vice President Strategic Programs, MosChip Technologies Limited.	:	Member
5.	Dr. Srinivasa Rao Zinka DGM Communication Systems, HBL Power Systems Ltd., Secunderabad.	:	Member
6.	Sri G. Vinay Kumar GM-Technical, Diqiloqic Systems Pvt. Ltd., Hyderabad.	:	Member
7.	Ms. Cherukuri Phani Madhuri Dy. Manager, IE, Bharat Electronics Ltd., Hyderabad.	:	Member
8.	Sri Siva Kumar Mamidisetti Signal processing Algorithm Lead, Unistring Tech Solutions Pvt. Ltd., Hyd.	:	Member
9.	Sri. Anand S. Moghe Formerly Vice-President (Engineering), M/s. Qualcore Logic Limited.	:	Special Invitee
10.	Dr. K. Veera Swamy, Professor, Dept of ECE, VCE.	:	Member
11.	Dr. Arun Kumar, Professor, Dept of ECE, VCE.	:	Member
12.	Dr. Srilakshmi Aouthu, Associate Professor, Dept of ECE, VCE.	:	Member
13.	Dr. D.M.K. Chaitanya, Associate Professor, Dept of ECE, VCE.	:	Member
14.	Mr. M. Prasanth, Assistant Professor, Dept of ECE, VCE.	:	Member
15.	Mrs. V. Aruna, Assistant Professor, Dept of ECE, VCE.	:	Member
16.	Dr. S. Aruna Deepthi, Assistant Professor, Dept of ECE, VCE.	:	Member
17.	Mr. V. Krishna Mohan, Assistant Professor, Dept of ECE, VCE.	:	Member
18.	Dr. Vibha D.K, Assistant Professor, Dept of ECE, VCE.	:	Member
19.	Dr. N. Abid Ali Khan, Assistant Professor, Dept of ECE, VCE.	:	Member
20.	Mrs. K.R. Deepthi, Assistant Professor, Dept of ECE, VCE.	:	Member
21.	Mr. K. Rama Krishna Reddy, Assistant Professor, Dept of ECE, VCE.	:	Member
22.	Mr. M. Ramanjaneyulu, Assistant Professor, Dept of ECE, VCE.	:	Member
23.	Mr. B. Uma Mahesh Babu, Assistant Professor, Dept of ECE, VCE.	:	Member
24.	Mrs. S. Jhansi Naga Laxmi, Assistant Professor, Dept of ECE, VCE.	:	Member
25.	Mr. K. Srikanth, Assistant Professor, Dept of ECE, VCE.	:	Member
26.	Mr. H. Shravan Kumar, Assistant Professor, Dept of ECE, VCE.	:	Member
27.	Mr. B. Srinivasa Rao, Assistant Professor, Dept of ECE, VCE.	:	Member
28.	Mr. Hafizuddin Mahmad, Assistant Professor, Dept of ECE, VCE.	:	Member
29.	Mr. K. Ramakrishna, Assistant Professor, Dept of ECE, VCE.	:	Member
30.	Mr. Punna Bharghava, Assistant Professor, Dept of ECE, VCE.	:	Member

The following members of Board of Studies could not attend the meeting.

1. Dr. Zafar Ali Khan Mohammed, Professor, Department of ECE, IIT-Hyderabad.
2. Dr. Sandeep Chaturvedi, Deputy General Manager, Head MMIC, GAETEC-DRDO, Hyderabad.
3. Sri. J. Sunil, CEO, Vaaluka Solutions Pvt. Ltd., Hyderabad.
4. Ms. G.R. Padmini, Associate Professor, Dept of ECE, VCE.
5. Dr. N.S.S. Reddy, Associate Professor, Dept of ECE, VCE.
6. Dr. K. Deepti, Associate Professor, Dept of ECE, VCE.
7. Dr. K. Krishna Kishore, Associate Professor, Dept of ECE, VCE.
8. Ms. R. Leelavathi, Assistant Professor, Dept of ECE, VCE.
9. Mrs. Ch. Neetu, Assistant Professor, Dept of ECE, VCE.
10. Dr. Ch. Vijaya Durga, Assistant Professor, Dept of ECE, VCE.

Dr. E. Sreenivasa Rao, Chairman BoS presided over the meeting. The following agenda items were taken up for discussion.

1. Welcoming the members.
   Chairman welcomed all the members to the 15th BoS meeting.

2. Confirmation of the minutes of 14th BoS meeting held on 24.6.2023.
   The minutes of the 14th meeting of the Board of Studies held on 24.6.2023 were read and confirmed.

3. Approval of the action taken report on the resolutions of the 14th BoS meeting held on 24.6.2023
   The following action taken report was reviewed and approved by the members:

Suggestions offered by the BoS member(s)	Action Taken		
Dr. B. Rajendra Naik, Professor, ECE Dept, OU-Hyd. He suggested to arrange some local Industry visits to 2nd and 3rd year students during semester breaks	Following local industrial visits were arranged for the students:		
	Name of the industry	Date of visit	Number of students visited
	NRSC, Jeedmetla, Hyderabad	26.3.2024	60 (IV-Sem.)
	NRSC, Shadnagar, Hyderabad	16.11.2023	60 (IV-Sem.)
	HBL Power Systems, Hyderabad	9.11.2023	6 (VII-Sem.)
	Astra Microwave Products Ltd. Hyderabad	10.10.2023	20 (VI-Sem.)
Sri. J. Sunil CEO, Vaaluka Solutions, Pvt. Ltd, Hyderabad • As there is no hostel facility in the campus, provide online cadence and other tools access to students through Internet/VPN, so that students will use the tools extensively for solving the Assignments, working on mini projects / Theme based projects/course projects/Major projects like IIITs, NITs and IITs. I told him that the department will explore the possibility of offering tools access not only to the students and but also to the faculty.	• VPN facility was established to provide students to access cadence and other tools.		

• Involve industry experts in course projects of Honours degree program to discuss problem statements, Methodology and in project review process. When I requested his support, he agreed to give his support in this process.	Sri. J. Sunil, CEO, Vaaluka Solutions, Pvt. Ltd, Hyderabad, has offered 10 problem statements on Design Verification related topics to the Honours students during VII-semester.
• He enquired about the availability of Verification IPs in cadence tools libraries. He said these IPs are very useful for verifying the Designs. I explained him that the department procured the Cadence standard bundle not the Research bundle which is very expensive. But I told him that I will discuss with vendor for possibility of getting access to the IPs.	• The Department requested the vendor (Entuple Technologies Ltd.) to provide the access to the IPs. But the vendor told that for Cadence University programme bundle, IPs cannot be provided. They inform that IPs have to be procured separately, if required.
Sri. Venkateswara Rao Somarouthu, Industry Representative, Director, AMD Hyderabad. • He said that under present situation, some of companies are planning to cut down the costs and ready to offer one year internships to B.E students during final year.	Chairman informed to the members that during VIII-Sem, students are available from Monday to Friday in a week for about 14 weeks, as they have online class work only on Saturdays.
Sri. Anand S Moghe, Former Vice President, Qualcore Logic Ltd Special Invitee • He suggested to include few topics in FPGA based system Design course in Honors program.	As per the suggestions of Sri. Anand S Moghe, the following FPGA performance parameters are included in FPGA Based System Design course (R-21). Maximum frequency calculation, set up & Hold time, Clock Skew, Jitter and Propagation Delay
Dr. D. Ranganadham Deputy Director General, Doordarshan Kendra, Vijayawada. Industry Representative • He enquired about the AI and ML based courses offered to the ECE students. Chairman explained the 2 AI and ML based courses introduced and offered to the students in Signal processing stream (Artificial Neural Networks and Image and Video processing using Machine Learning). He said he will go through the topics and offer suggestions	After going through the AI and ML based courses offered to ECE students, Dr. D. Ranganadham, suggested that there is a need to introduce a course on Language Models and Applications. Based on his suggestions, our faculty Mr. B. Uma Mahesh Babu & Prof. K. Veera Swamy proposed to introduce new professional elective course on Language Models and Applications in Signal Processing Stream.
Sri. Thati Rahul, Alumnus, Senior Systems Design Engineer, Xilinx India Technologies Pvt. Ltd., Hyderabad. He suggested that for Lateral Entry students, add one unit of OOPs topics in Programming Course in III-Sem, as these topics are very useful in system Verilog for Design Verification course.	As per the suggestions of Sri. Thati Rahul, our faculty have introduced OOPs concepts in Programming Techniques for Problem Solving Course for lateral entry students.

The chairman BoS, has informed the members that the department has implemented the above suggestions given by the members.

4. **Note on the department achievements.**
   Chairman has presented faculty, students and department achievements for the Academic Year 2023-24 to the members.

To review and recommend the Scheme of Instruction & Examination and Syllabi for all the semester of B.E (ECE), B.E (ECE) Honours and M.E (ES&VLSI Design) Programmes for the academic year 2024-25.

The Chairman has presented Scheme of Instruction & Examination as per the following agenda points to all the members.

5. a. Scheme of instruction & examination for B.E (ECE) I to VIII Semesters (R-24).
   b. Scheme of instruction & examination for B.E (ECE) Honors Degree Program in System on Chip Design.
   c. Syllabi for I and II semester courses (R-24).

6. Scheme of instruction & examination and syllabi for B.E (ECE) III & IV Semesters (R-23).

7. Scheme of instruction & examination and syllabi for B.E (ECE) V & VI Semesters (R-22).

8. Scheme of instruction & examination and syllabi for B.E (ECE) VII & VIII Semesters (R-21).

9. a. Scheme of instruction & examination for M.E (ES&VLSID) I to IV Semesters (R-24).

   b. Scheme of instruction & examination and syllabi for M.E (ES&VLSID) III & IV Semesters (R-23).

10. a. To review and finalize the stream based Open Electives to be offered to B.E (ECE) III to VI Semesters students for the academic year 2024-25.
    b. To review and finalize the stream based Professional Electives to be offered to B.E (ECE) VII semester (PE-I & PE-II Theory and Lab courses) & VIII Semester students for the academic year 2024-25.
    c. To review and finalize the Open Electives to be offered to M.E (ES&VLSID) students for the academic year 2024-25.
    d. To review and finalize the stream based Professional Electives to be offered to M.E (ES&VLSID) students for the academic year 2024-25.

After the deliberations, the members offered the following suggestions.

Name of the BoS member(s)	Suggestions offered
Dr. B. Rajendra Naik, Professor, ECE Dept, OU-Hyd.	• He enquired about the Department level alumni association activities. • He suggested to start Alumni local chapters and conduct activities on regular basis.
Dr. Sreehari Rao Patri Professor, Department of ECE, NIT-Warangal.	• He told that ECE Department, NIT Warangal is offering B.Tech. Electronics and Communication Engineering (VLSI Design and Technology) from A.Y. 2023-24. • He suggested to offer Python for Circuit Simulation as mandatory course for ECE students and consider to modify Engineering Drawing course as mandatory course without credits. Chairman informed that interested ECE students are taking Python programming as Open Elective course offered by CSE / IT Departments. • He also suggested to shift the VLSI Design theory and lab course from VII semester to V / VI semester. • He suggested to check if there is any redundancy / overlapped open elective courses with the courses offered in Minor degree program.

Name of the BoS member(s)	Suggestions offered
	Chairman informed that filters will be used during open elective registration process to block minor degree opted students to take the same open elective courses. • He also suggested the weightage of CIE can be changed from 40 to 60 marks. Chairman told that it will be discussed in academic committee meeting
Sri. D.V.R. Murthy Vice President Strategic Programs, MosChip Technologies Limited.	• He advised to start VLSI Design Club in ECE Department and arrange interaction / motivation sessions for juniors with seniors / alumni / working professionals on regular basis. • He also suggested to conduct FDP programmes on VLSI Design using Cadence Tools. Chairman informed that the department has organized an FDP on **"Analog and Digital IC Design Flow using Cadence Tools"** during 30th, 31st May, & 1st June, 2023, in association with Entuple Technologies Pvt. Ltd., Bangalore. Department is also planning another FDP on **Physical Design Flow using Cadence Tools** during next academic year. • He appreciated the chairman for introducing stream based professional elective theory and corresponding laboratory courses in VII semester, where students will get opportunity of their choice to explore any one of four different domains.

Dr. Srinivasa Rao Zinka
DGM Communication Systems, HBL Power Systems Ltd., Secunderabad.
	• He suggested to increase the focus on peripheral interfacing than architecture in Embedded Systems course.
	• He also suggested to introduce RTOS based experiments in Embedded Systems Lab.
	• He appreciated introducing the following experiments in Electronics Workshop Lab.
	  – Design of single layer PCB using EDA tools (Schematic, layout design & routing).
	  – Design of multilayer PCB using EDA tools (Schematic, layout design & routing).
	  – Introduction to 3D printing.
	  – Conversion of 3D model into 3D printing (Standard Triangle Language (STL) file conversion).
	He suggested to introduce one more experiment on understanding various specifications of component selection for PCB Design.
	• He suggested to introduce GUI based programming experiments using OOPS concepts in Python Open Elective Courses.
	• He also suggested to introduce GNU Radio based experiments in Analog and Digital Communication Lab.
	
	Chairman informed that the department will introduce GUI based programming experiments using OOPS concepts in C++ lab.
	
	The possibility of including GUI based programming experiments using OOPS concepts in Python Open Elective Courses will be discussed with CSE/IT HoDs.
	
	• He suggested to introduce SDR and its Applications elective course to M.E students also.

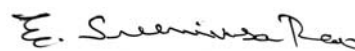| Name of the BoS member(s)	Suggestions offered
Sri G. Vinay Kumar GM-Technical, Diqiloqic Systems Pvt. Ltd., Hyderabad.	• He suggested to introduce experiments on NI based instruments to carryout measurements and testing. Chairman informed that the department will include myRIO and myDAQ NI based experiments • He also suggested to introduce hardware based experiments in Signals and Systems Lab apart from simulation based experiments.
Ms. Cherukuri Phani Madhuri Dy. Manager, IE, Bharat Electronics Ltd., Hyderabad.	• She suggested to introduce constraints based design and analysis experiments in labs and Mini Projects.
Sri Siva Kumar Mamidisetti Signal processing Algorithm Lead, Unistring Tech Solutions Pvt. Ltd., Hyd.	• He enquired about the initiatives adopted by the department to drive the students towards core job opportunities. Chairman informed that the following core companies are visiting the campus to recruit ECE students and will take necessary steps to attract core companies. MosChip Technologies, silicon labs, Vaaluka solutions, Smart SoC Solutions, Hyundai Mobis, Bosch, Qualcomm, Medha Sero Drives, ITC Badrachalam, Rodhe & Schwarz, AT&T Communication Services, UTS etc. • He suggested to introduce hardware based end-to-end DSP based experiments for complete understanding of the system. Chairman requested his support in this regard and he said he will help the faculty in setting up the experiments.
Sri. Anand S. Moghe Formerly Vice-President (Engineering), M/s. Qualcore Logic Limited. Special Invitee	• He said that Honours program curriculum is well designed and implemented by drawing Adjunct Faculty from industry.

Chairman has also discussed the scheme of instruction & examination of Minor Degree in Computer Science and Engineering to be offered by CSE Department for the students of Civil, Mech., EEE and ECE branches with additional 18 credits weightage.

After review and deliberations, the BoS recommended the proposed schemes & syllabi for B.E. (ECE), B.E (ECE) Honours Degree Program in System on Chip Design and M.E. (ES&VLSI Design) programmes for the academic year 2024-25.

11. Any other item with the permission of the chair.

▪ It is resolved that the Chairman and external BoS members attended the meeting will be signing all the approved schemes of UG & PG programmes, indicating the approval of the BoS.
▪ It is also resolved that the Chairman will be counter signing all the syllabi duly signed by the concerned faculty handling the courses of UG & PG programmes in ECE, indicating the approval of BoS.

The meeting concluded with a vote of thanks to the Chair.

(Dr. E. SREENIVASA RAO)
Chairman, BoS - ECE

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Copy to the Hon'ble CEO.
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