VASAVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

Ibrahimbagh, Hyderabad-31

Approved by A.I.C.T.E., New Delhi and

Affiliated to Osmania University, Hyderabad-07

Sponsored

by

VASAVI ACADEMY OF EDUCATION

Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR B.E. (ECE) VII and VIII Semesters

With effect from 2020-21

(For the batch admitted in 2017-18)

(R-17)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Phones: +91-40-23146040, 23146041

Fax: +91-40-23146090

Institute Vision

Striving for a symbiosis of technological excellence and human values

Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering

Department Mission

To inculcate a spirit of scientific temper and analytical thinking, and train the students in contemporary technologies in Electronics & Communication Engineering to meet the needs of the industry and society with ethical values

B.E (ECE) Program Educational Objectives (PEO's)	
PEO I	Graduates will be able to identify, analyze and solve engineering problems.
PEO II	Graduates will be able to succeed in their careers, higher education, and research.
PEO III	Graduates will be able to excel individually and in multidisciplinary teams to solve engineering and societal problems.
PEO IV	Graduates will be able to exhibit leadership qualities and lifelong learning skills with ethical values.

B.E. (ECE) PROGRAM OUTCOMES (PO's) Engineering Graduates will be able to:	
PO1	Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO2	Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO3	Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal and environmental considerations.
PO4	Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
P1O	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
P11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
P12	Lifelong learning: Recognize the need, and for have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

B.E (ECE) PROGRAM SPECIFIC OUTCOMES (PSO's)	
PSO I	ECE students will be able to analyze and offer circuit and system level solutions for complex electronics engineering problems, keeping in mind the latest technological trends.
PSO II	ECE students will be able to apply the acquired knowledge and skills in modeling and simulation of wireless communication systems.
PSO III	ECE students will be able to implement signal and image processing techniques for real time applications.

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) :: IBRAHIMBAGH, HYDERABAD – 500 031.
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION (R-17) :: B.E. - ECE : SEVENTH SEMESTER (2020 - 21)

B.E (ECE) VII - SEMESTER								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits
		Hours per Week			Duration in Hrs	Maximum Marks		
		L	T	P/D		SEE	CIE	
THEORY								
PC710EC	Microwave Engineering	3	-	-	3	60	40	3
PC720EC	VLSI Design	3	-	-	3	60	40	3
PE7XXEC	Professional Elective – I	3	-	-	3	60	40	3
PE7XXEC	Professional Elective – II	3	-	-	3	60	40	3
PE7XXEC	Professional Elective – III	3	-	-	3	60	40	3
PE7XXEC	Professional Elective – IV	3	-	-	3	60	40	3
PRACTICALS								
PC711EC	Microwave Engineering Lab	-	-	3	3	50	30	1
PC721EC	Electronic Design and Automation Lab	-	-	3	3	50	30	1
PW719EC	Project Seminar	-	-	2	-	-	30	1
	TOTAL	**18**	**-**	**8**		**460**	**330**	**21**
	GRAND TOTAL	**26**				**790**		

Professional Electives (R – 17) : Semester – VII		
Professional Elective – I		
1.	PE710EC	IoT Architectures and Protocols
2.	PE750EC	Mobile Cellular Communication
3.	PE790EC	DSP Processors and Architectures
4.	PE741EC	Wireless Sensor Networks
Professional Elective – II		
5.	PE720EC	Advanced Embedded Systems
6.	PE760EC	Optical Fiber Communication
7.	PE711EC	Speech and Audio Signal Processing
8.	PE751EC	Network Security
Professional Elective – III		
9.	PE730EC	Field Programmable Gate Arrays (FPGA) Architectures
10.	PE770EC	Coding theory and Techniques
11.	PE721EC	Digital Image and Video Processing
12.	PE761EC	Network Management
Professional Elective – IV		
13.	PE740EC	Electronic Instrumentation
14.	PE780EC	Satellite communication
15.	PE731EC	Biomedical Signal Processing
16.	PE771EC	Voice and Data Networks

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Microwave Engineering

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PC710EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Analyze the field components of waveguides 2. Understand the characteristics of Microwave sources and components	On completion of the course, students will be able to 1. Anlayse the E and H fields components of parallel and rectangular waveguides 2. Derive the characteristics of circular waveguides and cavity resonators 3. Analyse the scattering parameters of microwave components 4. Demonstrate the characteristics of Microwave sources 5. Describe the characteristics of microwave solid-state devices

UNIT-I :
Guided waves: Propagation of TE, TM and TEM waves between parallel planes. Velocity of propagation, wave impedance, attenuation in parallel plane guides.

UNIT-II:
Wave Guides: TE and TM waves in rectangular and circular wave-guides, Wave Impedance, Characteristic Impedance, Attenuation and Q of wave-guides. Cavity resonators, resonant frequency and Q, Applications of cavity resonator.

UNIT-III:
Microwave Circuits and Components: Concept of Microwave circuit, Normalized voltage and current, Introduction to scattering parameters and their properties, S parameters for reciprocal and Non-reciprocal components- Magic Tee, Directional coupler, E and H Plane Tees and their properties, Attenuators, Phase Shifters, Isolators and circulators.

UNIT-IV:

Microwave Tubes: High frequency limitations of conventional tubes, Bunching and velocity modulation, mathematical theory of bunching, principles and operation of two cavity, multi cavity, Reflex Klystron.

Theory of crossed field interaction; principles and operation of magnetrons and crossed field amplifiers, TWT and BWO.

UNIT-V:

Microwave Solid State Devices: Principles of operation, characteristics and applications of Varactor, PIN diode, GUNN diode and IMPATT diode, Elements of strip lines, micro strip lines, slot lines and finlines.

Learning Resources:

1. Samuel Y. Liao ,Microwave Devices and Circuits, 3rd ed, Pearson,2003
2. Edward C. Jordon, Keith G. Balmain, "Electromagnetic Waves and Radiating Systems", 15 June 2015, Pearson, 2nd Edition.
3. R.E. Collins, Foundations of Microwave Engineering, II edition, Wiley, 2001
4. K.C. Gupta Microwaves, John Wiley & Sons,1980
5. Annapurna Das, Sisir K. Das, Tata McGraw-Hill Education, 2000
6. https://swayam.gov.in/nd1_noc19_ee57
7. https://swayam.gov.in/nd1_noc19_ee68

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

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VLSI Design

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PC720EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To study the concepts of HDL and to model digital systems. 2 To understand the MOS fabrication technologies electrical properties and layout development of MOS circuits. 3 To analyze subsystem design concepts of adders and memories.	On completion of the course, students will be able to 1 Understand the concepts of modeling a digital system using Hardware Description Language. 2 Synthesize a digital system to meet design specifications of the system. 3 Have an understanding of the characteristics of CMOS circuit construction and the comparison between different state-of-the-art CMOS technologies. 4 Draw the stick and layout of basic digital design. 5 Design functional units including adders, shift registers and memories.

UNIT-I :

Introduction to HDLs, Basic Concepts of Verilog, Data Types, System Tasks and Compiler Directives. Gate Level Modeling: Gate Types and Gate Delays. Dataflow Modeling: Continuous assignment and Delays. Design of Stimulus Block.

UNIT-II:

Behavioural Modeling: Structured Procedures, Procedural Assignments, Timing control, Conditional statements, Sequential and Parallel Blocks, Generate Blocks. Switch level Modeling. Tasks, Functions, Procedural Continuous Assignments, Design of Mealy and Moore state models using Verilog. Logic Synthesis, Synthesis Design flow, Gate level Netlist.

UNIT-III:

Introduction to MOS Technology, Basic MOS Transistor action: Enhancement and Depletion Modes. Basic electrical properties of MOS, Threshold voltage and Body Effect. Design of MOS inverters with different loads, Basic Logic Gates with CMOS: INVERTER, NAND, NOR, AOI and OAI gates. Transmission gate logic circuits, BiCMOS inverter.

UNIT-IV:

MOS and CMOS circuit Design Process: MOS Layers, Stick diagrams, Lambda based Design rules and Layout diagrams. Basic Circuit Concepts: Sheet Resistance, Area Capacitance and Delay calculation.

UNIT-V:

Combinational Logic: Manchester, Carry select and Carry Skip adders, Crossbar and barrel shifters, Multiplexer.

Sequential Logic: Design of Dynamic Register Element, 3T, 1T Dynamic RAM Cell, 6T Static RAM Cell. D flip flop using Transmission gates. NOR and NAND based ROM Memory Design.

Learning Resources:

1. Samir Palnitkar, "Verilog HDL: A guide to Digital design and synthesis", 2/e, Pearson Education, 2008.
2. Michael D. Ciletti, "Advanced Digital Design with Verilog HDL", PHI, 2005.
3. Kamran Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, "Essentials of VLSI circuits and systems", PHI, 2011.
4. John P. Uyemura, "Introduction to VLSI Circuits and systems", John Wiley & Sons, 2011.
5. https://nptel.ac.in/courses/106105083/
6. https://nptel.ac.in/courses/106105165/
7. https://nptel.ac.in/courses/108107129/
8. https://nptel.ac.in/courses/117101058/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Microwave Engineering Lab

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:3	SEE Marks : 50	Course Code: **PC711EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Understand the basic characteristics of Microwave sources 2 Verify the relationship between guided wavelength and free space wavelength 3 Understand the measurement of various parameters of microwave components	On completion of the course, students will be able to 1 Describe the characteristics of microwave sources 2 Estimate the guide wave length and free space wave length 3 Measure the VSWR and impedance of unknown load 4 construct the scattering matrix of microwave junctions 5 Demonstrate characteristics of ferrite devices

Experiments:

1. Characteristics of Reflex Klystron oscillator
2. Characteristics of Gunn diode oscillator
3. Measurement of frequency and Guide wavelength calculation
4. Measurement of VSWR of a given load
5. Measurement of impedance
6. Scattering matrix of a Directional coupler.
7. Scattering matrix of Waveguide Tees: E plane, H plane
8. Scattering matrix of Magic Tee.
9. Characteristics of Isolator and its scattering matrix
10. Characteristics of Circulator and its scattering matrix
11. Calibration of attenuator at a given frequency
12. Calibration of frequency meter at a given frequency

New Experiments:

1. Radiation pattern measurement of an antenna
2. Analysis of rectangular wave guide.

Mini Project(s):

Simulation and Analysis of waveguide components

Learning Resources:

1. High frequency simulation software(HFSS)
2. Advanced Design Software(ADS)

The break-up of CIE :

1. No. of Internal Tests	:	1
2. Max. Marks for internal tests	:	10
3. Marks for day-to-day laboratory class work	:	15

Duration of Internal Tests: 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Electronic Design and Automation Lab

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:3	SEE Marks : 50	Course Code: **PC721EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To simulate and synthesize combinational & sequential logic circuits using EDA tools. 2. To learn implement procedure for any Digital design on FPGA.	On completion of the course, students will be able to 1. Familiarize the use of modern EDA tools to design digital logic circuits and system. 2. Apply the knowledge to develop Verilog HDL for digital circuits in various level of abstraction. 3. Develop stimulus block / Test bench in Verilog HDL to verify the functionality of design block. 4. Prototype digital hardware circuits using FPGA for real time application.

CYCLE - I Experiments

Write the Code using VERILOG, Simulate and synthesize the following

1. Arithmetic Units: Adders and Subtractors.
2. Multiplexers and Demultiplexers.
3. Encoders, Decoders, Priority Encoder and Comparator.
4. 8-bit parallel adder using 4-bit tasks and functions.
5. Arithmetic and Logic Unit with minimum of eight instructions.
6. Flip-Flops.
7. Registers/Counters.
8. Sequence Detector using Mealy and Moore type state machines.
9. Mini project

Note:-

1. All the codes should be implemented appropriately using Gate level, Dataflow and Behavioural Modelling.
2. All the programs should be simulated using test benches.
3. Minimum of two experiments to be implemented on FPGA/CPLD boards.

CYCLE - II Experiments

Transistor Level implementation of CMOS circuits

1 Basic Logic Gates: Inverter, NAND and NOR.
2 Half Adder and Full Adder.
3 4:1 Multiplexer.
4 2:4 Decoder.

New Experiments

1. Draw the layout for any complex CMOS logic and perform post-layout simulation.
2. Design of Memory using Verilog HDL.
3. Design of FIFO using Verilog HDL

The break-up of CIE : Internal Tests + Day to day Assignments

1.	No. of Internal Tests	:	1
2.	Max. Marks for internal tests	:	10
3.	Marks for day-to-day laboratory class work	:	15

Duration of Internal Tests: 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Project Seminar

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:3	SEE Marks : -	Course Code: **PW719EC**
Credits : 1	CIE Marks : 30	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. Selection of a suitable topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of project seminar report.

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.

Project seminar topics may be chosen by the student with advice and approval from the faculty members. Students are to be exposed to the following aspects of seminar presentation.

- Literature Survey
- Organization of the material
- Presentation of OHP slides / PC presentation
- Technical report writing

Each student is required to:

1. Submit a one-page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through OHP, PC, Slide project followed by a 10 minutes discussion.
3. Submit a report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

Students are required to submit a report on the project seminar.

- Batch size shall be 2 (or) 3 students per batch.
- Allocation by department.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project seminar report.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

IoT Architectures and Protocols

(Professional Elective-I)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE710EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The purpose of this course is to impart knowledge on IoT Architecture, practical constrains, various protocols and multiple case studies.	On completion of the course, students will be able to 1. Understand the Architectural Overview of IoT 2. Enumerate the need and the challenges in Real World Design Constraints 3. Choose the required protocol for a given application. 4. Explore IoT usage in various applications 5. Understand the Security requirements in IoT.

UNIT - I : IoT

Definition and Technologies that led to evolution of IOT, Characteristics of IoT, Physical Design of IoT, Logical Design of IoT, IoT Enabling Technologies, IoT Levels & Deployment. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT.

UNIT - II : IoT Reference Architecture

Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. IoT edge system architecture.

Real-World Design Constraints: Technical Design constraints, Connectivity constraints, Data representation and visualization, Big Data Management.

UNIT - III : IoT communications

Data link and physical layer Protocols: PHY/MAC Layer (IEEE 802.11, IEEE 802.15), Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy;
Network Layer Protocols: IPv4, IPv6, 6LoWPAN;
Transport layer protocols: TCP, MPTCP, UDP;
Messaging protocols: MQTT, CoAP, XMPP, DDS, AMQP.

UNIT - IV : Case Studies

Smart Cities, Smart Homes, Smart Transportation, Smart Healthcare, Precision Agriculture, Connected Vehicles.

IOT in Indian Scenario: i) IOT and Aadhaar ii) IOT for health services. iii) IOT for financial inclusion. iv) IOT for rural empowerment.

Industry 4.0: Industrial Internet of Things (IIoT), Reference Architecture, Characteristics of Industry 4.0.

UNIT - V : Securing the Internet of Things

Security Requirements in IoT Architecture - Security in Enabling Technologies, Security Concerns in IoT Applications.

Security Architecture in the Internet of Things - Security Requirements in IoT, Insufficient Authentication/Authorization, Insecure Access Control, Threats to Access Control, Privacy, and Availability, Attacks Specific to IoT.

Security and Vulnerabilities – Secrecy & Secret Key Capacity, Authentication/Authorization for Smart Devices, Transport Encryption, Secure Cloud/Web Interface, Secure Software/Firmware, Physical Layer Security.

Learning Resources:

1 Pethuru Raj and Anupama C. Raman, —The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press.

2 Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, —From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence‖, 1st Edition, 2014, Academic Press.

3 Arshdeep Bahga, Vijay Madisetti, —Internet of Things: A Hands-on Approach‖, Universities Press, 2014.

4 Practical Internet of Things Security (Kindle Edition) by Brian Russell, Drew Van Duren, Packt Publishing,2016.

5 Securing the Internet of Things Elsevier Authors: Shancang Li Li Da Xu,Paperback ISBN: 9780128044582,Imprint: SyngressPublished Date: 13th January 2017.

6 https://nptel.ac.in/courses/106105166/5

7 https://nptel.ac.in/courses/108108098/4

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Mobile Cellular Communication

(Professional Elective-I)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE750EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To provide fundamental principles and concepts required to understand the cellular communication systems and standards 2 To apply analytical techniques for characterization of wireless channel 3 To provide problem solving skills required to analyse and evaluate the performance of cellular communication systems.	On completion of the course, students will be able to 1 Demonstrate the fundamental design knowledge of cellular communication systems 2 Analyze different radio channel models and apply the knowledge acquired to formulate and solve problems. 3 Choose the proper multiple access scheme and modulation scheme depending on requirements of design. 4 Understand the evolution of cellular communication systems, architectures and standards 5 Become acquainted with recent advancements and developments in the area of mobile cellular communication and networking.

UNIT - I : Cellular system design concepts:

Basic Cellular system and its operation, frequency reuse, channel assignment strategies, Handoff process, factors influencing handoffs, handoffs in different Generations, Interference and system capacity, Enhancing capacity and cell coverage, Trunked radio system.

UNIT - II : Mobile Radio Wave propagation:

Large scale propagation models- Free space propagation model, three basic propagation mechanisms, practical link budget design using path loss models, outdoor propagation models-Durkin's model, indoor propagation model-partition losses. Small scale fading and multipath propagation, Parameters of mobile multipath channels, types of small scale fading.

UNIT - III : Multiple Access schemes and Modulation schemes:
FDMA, TDMA, Spread Spectrum Multiple Access- FHMA and CDMA, SDMA, Packet radio protocols-Pure ALOHA and Slotted ALOHA, CSMA, Reservation protocols, Modulation schemes- M-PSK, M-QAM, GMSK, Multicarrier modulation, OFDM.

UNIT - IV : Evolution of cellular systems:
Overview of cellular systems -1G, 2G , 2.5G, 3G and 4G. Wireless systems and standards- AMPS and ETACS, - GSM- Services, System architecture, Radio Sub system, Channel Types, Frame structure and Signal processing. CDMA features: IS-95 -Forward Channel, Reverse Channeling methods

UNIT - V : Beyond 2G cellular systems and Networking
Beyond 2G—GPRS and EDGE, Features and details of 3G systems-CDMA 2000, W-CDMA (UMTS) and HSPA, - Introduction to 4G systems—LTE and WiMAX, -WLAN systems, Bluetooth, PAN, Trends in Radio and Personal Communications.

Learning Resources:

1. Theodore.S. Rappaport, "Wireless Communications: Principles and Practice", 2/e, Pearson Education, 2010
2. William. C.Y.Lee, "Mobile Communication Engineering", 2/e , Mc-Graw Hill, 2011
3. Schwartz ,"Mobile Wireless Communications" Cambridge University Press, 2012
4. William stallings, "Wireless communications and networks" Pearson Education, 2/e, 2009
5. William. C. Y. Lee, "Mobile Cellular Telecommunications: Analog and Digital Systems", 2/e, Mc-Graw Hill, 2011.
6. https://nptel.ac.in/courses/106106167/
7. Introduction to cellular and wireless communications- by Dr. David.K, IITM
8. https://www.coursera.org/learn/wireless-communications
9. https://www.udemy.com/introduction-to-wireless-communications/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DSP Processors and Architectures

(Professional Elective-I)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE790EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To give an exposure to the fixed point point DSP architectures and to implement various signal processing algorithms using TI DSPs.	On completion of the course, students will be able to 1 Differentiate between DSP Processors and General Purpose processors. 2 Apply different number formats on DSP processors 3 Understand the architecture details of fixed point & floating point DSPs. 4 Illustrate the features of on-chip peripherals and its interfacing with DSP processors. 5 Design and implement signal processing algorithms on DSP processors.

UNIT - I : Number Format Representation and Source of Errors

Introduction, Digital signal processing system, Differences between DSP and other micro processor architectures. Fixed point, Floating point and block Floating point formats, IEEE-754 Floating point, Dynamic range and precision, Sources of error in DSP implementations, A/D Conversion errors, D/A Conversion Errors, Q-notation.

UNIT - II : Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Special addressing modes, Address Generation Unit, Programmability and Program Execution, Speed Issues, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects.

UNIT - III : Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX

Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT - IV : Floating point DSPs

Types of Floating point DSPs, Features of TMS320C67XX Processors, Architecture of 'C67X Processor-CPU, General Purpose Registers files, Functional Units and Operation, Data paths, Control Register File, Addressing modes-Register, Linear & Circular addressing modes, Instructions set-Fixed and Floating point instructions, Pipelining and on-chip peripherals.

UNIT - V : Implementations of Basic DSP Algorithms & Interfacing of 'C54xx

FIR Filters, IIR Filters, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example, An Image Processing System.

Learning Resource:

1. Avtar Singh, S. Srinivasan "Digital Signal Processing Implementations: Using DSP Microprocessors--With Examples from TMS320C54xx", Cengage Learning (2004)
2. B. Venkataramani, M. Bhaskar, "Digital Signal Processors, Architecture Programming and Applications", Tata Mc Graw Hill, 2013.
3. Lapsley et al. "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.
4. Rulph Chassaing, "Digital Signal Processing and Applications with the C6713 and C6416 DSK", John wiley & sons, 2005.
5. Digital Signal Processing: A practical approach, Ifeachor E. C., Jervis B. W Pearson Education, PHI/ 2002
6. "Architectures for Digital Signal Processing", Peter Pirsch John Weily, 2007.
7. Jonatham Stein, "Digital Signal Processing", John Wiley, 2005.
8. https://nptel.ac.in/courses/108102045/8

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Wireless Sensor Networks

(Professional Elective-I)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE741EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Differentiate WSNs and mobile ad-hoc networks and illustrate the single node computational blocks and design challenges narrating WSN fundamental entities. 2 Analyze and Summarize the MAC (L-2) and Routing (L-3) protocols along with the physical transceiver radio design. 3 Describe WSN topology, localization along with existing hardware support and software simulators and programming models.	On completion of the course, students will be able to 1 Synthesize Wireless Sensor Network Characteristics and its challenges; and, differentiate WSN with other ad-hoc networks. 2 Illustrate architecture of Single WSN mote with Energy consumption mathematical models of a single mote both during the transmission and reception. 3 Differentiate Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks and their comparisons 4 Study different topology control and clustering schemes with localization concepts. 5 Mention some of the widely used WSN simulation tools and platforms with engineering case studies.

UNIT - I : OVERVIEW OF WIRELESS SENSOR NETWORKS

Challenges for Wireless Sensor Networks Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- Enabling Technologies for Wireless Sensor Networks

UNIT - II : ARCHITECTURES

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concept

UNIT - III : NETWORKING SENSORS

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC, Zigbee: IEEE 802.15.4 MAC Layer, The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

UNIT - IV : INFRASTRUCTURE ESTABLISHMENT

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT - V : SENSOR NETWORK PLATFORMS AND TOOLS

Operating Systems for Wireless Sensor Networks, Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms, Node-level Simulators, State-centric programming.

Learning Resource:

1. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks," John Wiley, 2005.
2. Feng Zhao and Leonidas J. Guibas, “Wireless Sensor Networks - An Information Processing Approach," Elsevier, 2007.
3. Kazem Sohraby, Daniel Minoli, and Taieb Znati, “Wireless Sensor Networks-Technology, Protocols and Applications,” John Wiley, 2007.
4. Anna Hac, “Wireless Sensor Network Designs,” John Wiley, 2003.
5. https://nptel.ac.in/courses/106105160/21

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Embedded Systems

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code : **PE720EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Define and classify embedded system and to interpret design process and challenges. 2 Summarize the RISC concepts and describe the ARM architecture, Interpret serial and parallel bus communication protocols. 3 Describe system design and co-design issues along with various laboratory, IDE tools and design case studies.	On completion of the course, students will be able to 1 Define embedded system & describe the embedded system product design life cycle and challenges. 2 Analyse the ARM Core embedded design and its programming model. 3 Apply knowledge to design networked embedded systems using serial, parallel and wireless communication protocols. 4 Justify the importance of hardware software co-design and models involved. 5 Acquire the knowledge of embedded IDEs to design and specify debugging techniques.

UNIT – I : Embedded System Design

Introduction, Trends, Definition, Classifications; Embedded Product Development Life Cycle. CPU selection–hardware, software, memories and I/O. Challenges in designing Embedded System; Design Metric of Embedded System.

UNIT - II: ARM Processor Fundamentals

Nomenclature; Core Architecture; AMBA Bus–ASB, APB; Registers; operating modes; Pipeline; Introduction to Thumb Mode; Exceptions, OBD using JTAG; ARM Core Revisions and comparisons; Overview of Cortex Cores; Case Study of LPC2148 & LPC1768 (Qualitative Analysis Only)

UNIT - III: Embedded Networking

Traditional Networking Vs Embedded Networking; issues involved; Networking through serial protocols: UART, I2C, SPI, CAN, IEEE1394 and USB; PCI for embedded systems.

Porting of TCP/IP: Socket selection; HTTP client-server model; Design considerations; example case study of embedded web server.

Porting Wireless Networking Stacks: WiFi; BLE; Zigbee; GSM/GPRS; 3G/4G–issues and design considerations.

UNIT - IV: Hardware Software Co-Design

Single-processor and Multi-Processor Architectures, comparison of Co-Design Approaches; Formulation of the HW/SW scheduling, Optimization of Design Metric: Case study of Embedded Adaptive Cruise Control Design.

UNIT - V: Embedded Software Architectures & Debugging Methods

Embedded Software Development Tools: Host and Target machines, native tools–IDEs; cross-compilers, GCC

Embedded Software Architectures: Round Robin, RR with Interrupt driven, Functional Queue and introduction to RTOS.

Debugging Methods: Testing on Host–Instruction set Simulators, ICE, JTAG, laboratory tools: Multi meter, CRO, Logic Analyzer & protocol sniffers.

Learning Resource:

1 Tony Givargis Frank Vahid "Embedded System Design: A Unified Hardware/Software Introduction" Wiley Student Edition, 2006
2 Andrew Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Morgan Kaufmann Publishers In, 2004
3 Marilyn Wolf, "Computers as Components: Principles of Embedded Computing Systems Design", Elsevier; Third edition (2013)
4 NPTEL Course: Prof. Indranil Sen Gupta, Dr. Kamalika Datta, IIT Kharagpur, "Embedded System Design with ARM" https://nptel.ac.in/noc/individual_course.php?id=noc19-cs22

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Test	: 20
2. No. of Assignments	: 3	Max. Marks for each Assignment	: 5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	: 5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Optical Fiber Communication

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE760EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize with the optical sources, detectors and optical communication links.	On completion of the course, students will be able to 1 Understand the principles fiber-optic communication, the components and the bandwidth advantages. 2 Understand the properties of the optical fibers and optical components. 3 Understand operation of optical sources and detectors. 4 Analyze system performance of optical communication systems. 5 Design optical networks and understand non-linear effects in optical fibers.

UNIT – I:

Introduction to vector nature of light, propagation of light, propagation of light in a cylindrical dielectric rod, Ray model, wave model.

UNIT - II:

Different types of optical fibers, Modal analysis of a step index fiber.
Signal degradation on optical fiber due to dispersion and attenuation. Fabrication of fibers and measurement techniques like OTDR.

UNIT - III:

Optical sources - LEDs and Lasers, Photo-detectors - pin-diodes, APDs, detector responsivity, noise, optical receivers. Optical link design - BER calculation, quantum limit, power penalties.

UNIT - IV:

Optical switches - coupled mode analysis of directional couplers, electro-optic switches. Optical amplifiers - EDFA, Raman amplifier. WDM and DWDM systems. Principles of WDM networks

UNIT - V:

Nonlinear effects in fiber optic links. Concept of self-phase modulation, group velocity dispersion and solition based communication.

Learning Resources:

1 J. Keiser, Fibre Optic communication, McGraw-Hill, 5th Ed. 2013 (Indian Edition).
2 G. Agrawal, Fiber optic Communication Systems, John Wiley and sons, 3rd Ed, 2002.
3 K.C. Gupta, Opto Electronic Devices and Systems, PHI Learning, 2005.
4 https://nptel.ac.in/courses/117101054/
5 https://nptel.ac.in/courses/117104127/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Speech and Audio Signal Processing

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE711EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the mechanism of speech production. 2 To analyze various speech synthesizers. 3 To study various types of coders and decoders. 4 To analyze speaker identification and verification systems.	On completion of the course, students will be able to 1 Apply the knowledge of science to design an artificial model of speech production system. 2 Analyse the types of speech signals & convert the signals to digital. 3 Synthesize the speech signal using a text as input. 4 Design speech encoder and decoder. 5 Also design an Automatic speech recognition system (ASR) by pattern matching method.

UNIT - I :

Applications of Digital Speech Processing, Phonetic Representation of Speech, Models for Speech Production-Schematic model of the vocal tract system, Source filter model for a speech signal production. Speech Quantization- Scalar quantization–uniform quantizer, optimum quantizer, logarithmic quantizer, adaptive quantizer, differential quantizers; Vector quantization.

UNIT - II :

Short-Time Analysis of Speech-Short-Time Energy and Zero-Crossing Rate, Short-Time Autocorrelation Function (STACF), Short-Time Fourier Transform (STFT), The Speech Spectrogram, Relation of STFT to STACF. Pitch-period estimation Homomorphic Speech Analysis.

UNIT - III :

Speech Synthesis Methods, Linear predictive synthesizer, phone use synthesis, Introduction to Text-to-Speech and Articulator speech synthesis.

UNIT - IV :

Sub-band coding, Transforms coding, channel decoder, Formant decoder, Cepstral decoder, linear predictive decoder, vector quantizer coder.

UNIT - V :

Automatic Speech Recognition (ASR), The Problem of Automatic Speech Recognition, Building a Speech Recognition System, The Decision Processes in ASR ,Representative Recognition Performance, Challenges in ASR Technology.

Learning Resources:

1. Lawrence R. Rabiner and Ronald W. Schafer, "Introduction to Digital Speech Processing", now, 2007.
2. Owens F.J., "Signal Processing of Speech", Macmillan, 2000.
3. Daniel Jurefskey & James H. Martin, "Speech and Language Processing", Pearson Education, 2003.
4. https://nptel.ac.in/courses/117105145/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Network Security

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE751EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To acquire knowledge on standard algorithms used to provide confidentiality, integrity and authenticity. 2 To understand the various key distribution and management schemes and to deploy encryption techniques to secure data in transit across data networks.	On completion of the course, students will be able to 1 Analyze the vulnerabilities in any computing system and hence be able to design a security solution 2 Identify the security issues in the network and resolve it. 3 Evaluate security mechanisms using rigorous approaches 4 Analyze network security and web security requirements. 5 Illustrate the applications in network security

UNIT - I :

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security, Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques. Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Block Cipher Design Principles.

UNIT - II :

Encryption: Triple DES, International Data Encryption algorithm, Characteristics of Advanced Symmetric block ciphers. Conventional Encryption Placement of Encryption function

UNIT - III :

Public Key Cryptography Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange , Number Theory in brief.

UNIT - IV :

Message Authentication and Hash Functions Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME

UNIT - V :

IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms: Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems

Learning Resources:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.
3. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
4. https://nptel.ac.in/courses/106105031/

The break-up of CIE : Internal Tests + Assignments + Quizzes

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2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Field Programmable Gate Arrays (FPGA) Architectures

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE730EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize the students with the designing aspects of FPGA's utilizing digital design techniques.	On completion of the course, students will be able to 1 Differentiate between ROM, PAL, PLA, SPLD, CPLD, and FPGA. 2 Understand working of building blocks of FPGA 3 Compare the features of Various FPGAs in terms of their Architecture, Configurable logic block. 4 Gain knowledge on routing algorithms adopted in FPGAs. 5 Test a particular PLD using various techniques like design validation, Timing verification.

UNIT - I: Introduction to PLD's and PGA'S

Memory- Read-only memory, read/write memory - SRAM and DRAM. Programmable Logic Devices-PLAs, PALs and their applications; Sequential PLDs and their applications; State- machine design with sequential PLDs; Programmable gate arrays (pgas), Introduction to field programmable gate arrays (FPGAs),design flow using FPGA, programming technologies.

UNIT - II: FPGA Architctural Aspects

Field Programmable Gate Arrays: Organization of FPGAs, Programmable Logic Block Architectures, Programmable Interconnect, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs

Logic Block Architectures: Logic block functionality versus area-efficiency, Logic block area and routing model, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT - III: FPGA Architectures and comparision

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, virtexII FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT - IV: Placement and Routing Algorithms in FPGA Architectures

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT - V:Testing methods in FPGA Architectures

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps.Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Learning Resources:

1 S. Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 1994.
2 John V.Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 1995.
3 P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
4 S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
5 https://nptel.ac.in/syllabus/117108040/prof.Kuruvilla Varghese IISC Banglore

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Coding Theory and Techniques

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE770EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the process of digital transmission 2 To study different error control techniques in digital transmission 3 To apply encoding and decoding techniques	On completion of the course, students will be able to 1 Apply the probabilistic method to construct different types of source codes. 2 Identify different types of errors and to comprehend various error control code properties. 3 Apply linear block codes and convolution codes for error detection and correction. 4 Generate LDPC codes using Gallager's method of construction and to demonstrate the BER performance of LDPC codes. 5 Construct Galois Fields and to apply them to generate BCH and RS codes for Channel performance improvement against burst errors.

UNIT - I:

Introduction : Coding for Reliable Digital Transmission and Storage, Types of codes, Modulation and Coding, Maximum Likelyhood Decoding, Types of errors, Source coding: Shannon-Fano coding, Huffman codes, Run-Length Encoding, Lampel-Ziv codes.

UNIT - II:

Block codes : Important Linear Block Codes, Repetition codes, Hamming codes, a class of single error-correcting and double-error correcting codes, Reed-Muller codes, the (24,12) Golay code, Product codes, Interleaved codes.

UNIT - III:

Convolutional codes : Encoding, Structural properties, State diagram, Code tree diagram, Maximum-Likelihood decoding, Soft decision and hard decision decoding, the Viterbi algorithm.

UNIT - IV:

Low Density Parity Check codes : Introduction, Galleger's method of construction, Regular and Irregular LDPC codes, other methods of constructing LDPC codes, Tanner graphs, Decoding of LDPC codes.

UNIT - V:

BCH and RS codes : Groups, Fields, Binary arithmetic, Construction of Galois Fields GF(2^m), Basic properties of Galois Fields, Introduction to BCH and RS codes.

Learning Resource:

1. Shu Lin and Daniel J. Costello, Jr. "Error Control Coding," 2/e, Pearson, 2011.
2. K Sam Shanmugum, "Digital and Analod Communication Systems," Wiley, 2010.
3. Simon Haykin, "Digital Communication," TMH, 2009.
4. https://nptel.ac.in/courses/117106031/

The break-up of CIE : Internal Tests + Assignments + Quizzes

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2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Digital Image and Video Processing

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE721EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the elements of digital image processing and note its importance in various applications. 2 To acquire the knowledge on image transforms to be implemented for image enhancement, image restoration and image compression. 3 To study various coding techniques being used.	On completion of the course, students will be able to 1 Mathematically represent the various types of images and analyze them. 2 Process these images for the enhancement of certain properties or for optimized use of the resources. 3 Develop algorithms for image compression and coding 4 Extract required information from image by image segmentation techniques. 5 Represent and process video to extract information

UNIT - I:

Digital Image Fundamentals-Elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels – neighborhood, adjacency, connectivity, distance measures.

UNIT - II:

Fourier transform, FFT, Discrete cosine transform, Hadamard transform, Haar transform, Slant transform and Hotelling transform and their properties. Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT - III:

Spatial enhancement techniques: Histogram equalization, direct histogram specification, Local enhancement.

Frequency domain techniques: Low pass, High pass and Homomorphic Filtering, Image Zooming Techniques. Image Degradation model,

Algebraic approach to restoration, inverse filtering, Least mean square filter, Constrained least square restoration and interactive restoration. Speckle noise and its removal techniques.

UNIT - IV:

Image Compression-Redundancy–inter-pixel and psycho-visual, Huffman Coding, Arithmetic coding, Bit-plane coding, Lossless compression – predictive, Lossy compression-predictive and Transform coding techniques: Zonal coding and Threshold coding, Image Segmentation-Detection of discontinuities, edge linking and boundary detection, thresholding – global and adaptive, region-based segmentation.

UNIT - V:

Video formation, perception, and representation ,two dimensional motion estimation

Learning Resources:

1 R.C. Gonzalez and R.E. Woods, Digital Image Processing, third Edition,Pearson.
2 Education 4th edition 2018 Anil Kumar Jain, Fundamentals of Digital Image Processing, Prentice Hall of India.2nd edition 2004.
3 Video Processing and Communications Yao Wang, Jorn stermann, and Ya-Qin Zhang Prentice Hall, 2002 (Published September 2001).
4 Murat Tekalp , Digital Video Processing" Prentice Hall, 2nd edition 2015.
5 http://nptel.ac.in/courses/117105079
6 http://nptel.ac.in/courses /117104020

The break-up of CIE : Internal Tests + Assignments + Quizzes

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2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Network Management

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE761EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize the students with the network architectures and management issues.	On completion of the course, students will be able to 1. Explain network management perspectives 2. Apply various network management protocol 3. Identify and describe TMN standards 4. Analyze various management issues 5. Demonstrate how to correctly maintain LAN

UNIT - I:

Overview of Data Communication and Network Management – Goals, Organization and Functions; Network Management – Architecture and Organization; Network Management Perpestives; Current Status and Future of Network Management. Network Topology, Network Node Components, Transmission Technology.

UNIT - II:

Network Management Standards, Network Management Models, Organizational Model, Information Model, Communication Model. **SNMPv1 –**History of SNMP, Internet Organization and Standards, SNMP Model, Organizational Model, System Overview, Information Model. SNMP Communication Model, Functional Model.SNMPv2 and SNMv3.

UNIT - III:

TMN Conceptual Model, TMN Standards, TMN Architecture, TMN Management Service Architecture, TMN Integrated View, TMN Implementation.

UNIT - IV:

Configuration Management, Fault Management, Performance Management, Security Management, Service Level Management, Accounting Management, Report Management, Policy-Based Management.

UNIT - V:

Setting-UP LAN Access, SNMP configuration, Switched Port Analyzer, Web Browser / Web Server Communication.IP Network Management – Configuration, Management Information Base, Simple Network Management Protocol, IP-Based Service Implementation- Network Management Issues, OSS Architecture.

Learning Resources:

1. Mani Subramanian "Network Management – Principles and Practice", Addison-Wesley, 2000.
2. Salah Aiidarons, Thomas Plevayk, "Telecommunications Network Technologies and Implementations", Eastern Economy Edition IEEE press, New Delhi, 1998.
3. Lakshmi. G, Raman, "Fundamentals of Telecommunication Network Management", Eastern Economy Edition IEEE Press, New Delhi
4. J. Richard Burke, "Network Mamagement: Concepts and Practice, A Hands-on Approach ", Pearson Education, 2008.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Electronic Instrumentation

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE740EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Explain basic concepts and definitions in measurement. 2 Elaborate discussion about the importance of signal generators and analyzers in Measurement. 3 provide a brief knowledge of measurements and measuring instruments related to engineering	On completion of the course, students will be able to 1 Identify different characteristics of instruments and errors in measurements. 2 To use modern instruments for measurements. 3 Demonstrate working principle and usage of medical instruments. 4 Modeling of various applications in virtual instrumentation. 5 Analyze various voltmeters, CRO, spectrum analyzer.

UNIT – I

Accuracy, Precision, Resolution and Sensitivity. Errors and their types. Standards of measurement, classification of standards, IEEE standards, Elements of ISO 9001, Quality management standards.

UNIT – II

Transducers: classification, factors for selection of a transducer, transducers for measurement of velocity, acceleration, force, radio activity, Hot wire anemometer. Passive electrical transducers- Strain gauges and strain measurement, LVDT and displacement measurement, capacitive transducer and thickness measurement. Active electrical transducers: Piezo electric, photo conductive, photo voltaic and photo emissive transducers.

UNIT – III

Characteristics of sound, pressure, power and loudness measurement. Microphones and their types. Temperature measurement, resistance wire thermometers, semiconductor thermometers and thermocouples. Humidity measurement, resistive capacitive, aluminum oxide and crystal Hygrometer types.

UNIT – IV

Block diagram, specification and design considerations of different types of DVMs. Digital LCR meters, Spectrum analyzers. The lEEE488 or GPIB Interface and protocol.

Delayed time base oscilloscope, Digital storage oscilloscope, and mixed signal oscilloscope. Introduction to virtual instrumentation, SCADA. Data acquisition system block diagram

UNIT-V

Biomedical Instrumentation: Human physiological systems and related concepts. Bio-potential electrodes Bio-potential recorders - ECG, EEG, EMG, X- ray machines and CT scanners, magnetic resonance and imaging systems, Ultrasonic Imaging systems.

Learning Resources:

1 Albert D. Helfric, and William D. Cooper, "Modern Electronic Instrumentation and Measurement Techniques", PHI, 2010.
2 H S Kalsi, "Electronic Instrumentation", 3/e, TMH, 2011.
3 Nakra B.C, and Chaudhry K.K., "Instrumentation, Measurement and Analysis", TMH, 2004
4 Khandpur. R.S., "Handbook of Bio-Medical Instrumentation", TMH, 2003.
5 https://nptel.ac.in/courses/108105064

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Satellite Communication

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE780EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the working principles of various satellites and their importance in global communication 2 To acquire the knowledge on satellite sub systems and various factors affecting the function of communication satellite. 3 To study the need of multiple access techniques and various protocols being used in satellite communications	On completion of the course, students will be able to 1 Understand the importance of satellite communication systems and various types of satellites 2 Explain satellite subsystems telemetry, tracking and command control. 3 Calculate various parameters of satellite. 4 Describe purpose of special communication satellites, need of various multiple access techniques. 5 Analyze the performance of special purpose communication satellite.

UNIT – I

Evolution and growth of communication satellites, synchronous satellites, frequency allocation, orbits, orbital mechanism and kepeler's law and velocity, effects of orbital inclination, azimuth and elevation, coverage angle and slant range, eclipse, placements of a satellite in geo-stationery orbit.

UNIT – II

Space segment, stabilization, communication subsystems, Telemetry, tracking and command Attitude & orbital Control Systems, Power Systems, earth segment, earth station, large and small earth station antennas, parabolic reflectors, Newtmian assegrain and Gregorian feed arrangements, offset feed, HPAs and LNAs, redundancy configuration., Thermal System.

UNIT - III

System noise temperature and G/T ration, Basic RF link analysis, EIRP, C/N, Interference, attenuation due to rain, cross polarization, design of uplink and down link

UNIT - IV

Multiple access techniques, FDM-FM-FDMA, SCPC companded systems, TDMA frame structure, Frame efficiency, superframe structure, frame acquisition and synchronization, types of demand assignments, DAMA characteristics, SPADE.

UNIT - V

Special purpose communication satellites, DBS, INTELAST, INMARSAT, MSAT, VSAT, LEO, Global positioning system, Echo- Cancellation techniques, Protocols, HDLC, Satellite applications, Indian activities in satellite communication, APPLE, INSAT-1, INSAT-2.

Learning Resources:

1. Tri-T-ha, Digital Satellite Communications, 2nd Edition, McGraw Hill, 1990.
2. Dr. D.C Agarwal, Satellite Communications 4th Edition, Khanna Publishers, 1996
3. Timothy Pratt and Charles W. Bostan, Satellite Communications, 1986.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Biomedical Signal Processing

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE731EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To introduce the fundamentals of probability theory and random processes with biomedical signals applications. 2 To equip students with the fundamental tools that are used to describe, analyze and process biomedical signals. 3 To acquire the knowledge on fundamental principles in the analysis and design of filters, power spectral density estimation and non-stationary signal processing techniques with cardiological and neurological signals.	On completion of the course, students will be able to 1 Apply the probability theory and random processes techniques in analyzing biological signals. 2 Determine to best class of compression techniques to use for a particular bio medical signal to compress. 3 Possess the basic mathematical, scientific and computational skills necessary to analyze and process cardiological signals as per the requirement. 4 Ability to formulate and solve basic problems in biomedical signal analysis. 5 Possess the basic mathematical, scientific and computational skills necessary to analyze and process neurological signals as per the requirement..

UNIT – I

Discrete and continuous Random variables: Probability distribution and density functions. Gaussian and Rayleigh density functions, Correlation between random variables.

Stationary random process, Ergodicity, Power spectral density and autocorrelation function of random processes. Noise power spectral density analysis, Noise bandwidth, noise figure of systems.

UNIT – II

Data Compression Techniques: Lossy and Lossless data reduction Algorithms. ECG data compression using Turning point, AZTEC, CORTES, Huffman coding, vector quantisation, DCT and the K L transform.

UNIT – III

Cardiological Signal Processing: Pre-processing. QRS Detection Methods. Rhythm analysis. Arrhythmia Detection Algorithms. Automated ECG Analysis. ECG Pattern Recognition. Heart rate variability analysis.
Adaptive Noise Cancelling: Principles of Adaptive Noise Cancelling. Adaptive Noise Cancelling with the LMS Adaptation Algorithm. Noise Cancelling Method to Enhance ECG Monitoring. Fetal ECG Monitoring.

UNIT – IV

Signal Averaging, polishing – mean and trend removal, Prony's method, Prony's Method based on the Least Squares Estimate, Linear prediction. Yule – walker (Y –W) equations, Analysis of Evoked Potentials.

UNIT-V

Neurological Signal Processing: Modelling of EEG Signals. Detection of spikes and spindles Detection of Alpha, Beta and Gamma Waves. Auto Regressive (A.R.) modelling of seizure EEG. Sleep Stage analysis. Inverse Filtering. Least squares and polynomial modelling.

Learning Resources:

1. Probability, Random Variables & Random Signal Principles – Peyton Z. Peebles, 4th ed., 2009, TMH.
2. Biomedical Signal Processing- Principles and Techniques - D.C.Reddy, 2005, TMH.
3. Digital Bio signal Processing - Weitkunat R, 1991, Elsevier.
4. Biomedical Signal Processing - Akay M, IEEE Press.
5. Biomedical Signal Processing -Vol. I Time & Frequency Analysis - Cohen.A, 1986, CRC Press.
6. Biomedical digital Signal Processing: C-Language Experiments and Laboratory Experiments, Willis J.Tompkins, PHI.
7. https://nptel.ac.in/courses/108105101/ Biomedical Signal Processing - by Prof.Sudipta Mukhopadhyay. IITKGP
8. http://www.ecdept.iitkgp.ac.in/index.php/home/faculty/smukho

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Voice and Data Networks

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE771EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To introduce students to the concepts of Voice & Data Networks.	On completion of the course, students will be able to 1 Design Voice and Data Networks. 2 Apply switching techniques. 3 Apply protocols corresponding to various layers 4 Design sub netting 5 Analyze various networks issues

UNIT – I

Network Design Issues, Network Performance Issues, Network Terminology, centralized and distributed approaches for networks design, Issues in design of voice and data networks.

UNIT – II

Layered and Layer less Communication, Cross layer design of Networks, Voice Networks (wired and wireless) and Switching, Circuit Switching and Packet Switching, Statistical Multiplexing.

UNIT – III

Data Networks and their Design, Link layer design- Link adaptation, Link Layer Protocols, Retransmission. Mechanisms (ARQ), Hybrid ARQ (HARQ), Go Back N, Selective Repeat protocols and their analysis.

UNIT – IV

Queuing Models of Networks, Traffic Models, Little's Theorem, Markov chains, M/M/1 and other Markov systems, Multiple Access Protocols, Aloha System , Carrier Sensing, Examples of Local area networks,

UNIT-V

Inter-networking, Bridging, Global Internet, IP protocol and addressing, Sub netting, Classless Inter domain Routing (CIDR), IP address lookup, Routing in Internet. End to End Protocols, TCP and UDP. Congestion Control, Additive Increase/Multiplicative Decrease, Slow Start, Fast Retransmit/ Fast Recovery, Congestion avoidance, RED TCP Throughput Analysis, Quality of Service in Packet Networks.Network Calculus, Packet Scheduling Algorithms.

Learning Resources:

1. D. Bertsekas and R. Gallager, "Data Networks", 2nd Edition, Prentice Hall, 1992.
2. L. Peterson and B. S. Davie, "Computer Networks: A Systems Approach",5th Edition, Morgan Kaufman, 2011.
3. Kumar, D. Manjunath and J. Kuri, "Communication Networking: An analytical approach", 1st Edition, Morgan Kaufman, 2004.
4. Walrand,"Communications Network: A First Course", 2nd Edition, McGraw Hill, 2002.
5. Leonard Kleinrock, "Queueing Systems,Volume I: Theory", 1st Edition, John Wiley and Sons, 1975.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) :: IBRAHIMBAGH, HYDERABAD – 500 031.
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION (R-17) :: B.E. - ECE : EIGHTH SEMESTER (2020 - 21)

B.E (ECE) VIII - SEMESTER								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits
		Hours per Week			Duration in Hrs	Maximum Marks		
		L	T	P/D		SEE	CIE	
THEORY								
PE8XXEC	Professional Elective – V	3	-	-	3	60	40	3
PE8XXEC	Professional Elective – VI	3	-	-	3	60	40	3
PRACTICALS								
PW819EC	Project Work / Internship	-	-	18	Viva-Voce	50	50	9
	TOTAL	**6**	**-**	**18**		**170**	**130**	**15**
	GRAND TOTAL	**24**				**300**		

Professional Electives (R – 17) : Semester – VIII		
Professional Elective – V		
1	PE810EC	Low Power VLSI Design
2	PE830EC	Global Positioning System
3	PE850EC	Image and Video processing using Machine Learning
4	PE870EC	Optical Networks
Professional Elective – VI		
5	PE820EC	Real Time Systems
6	PE840EC	Radar and Navigation Systems
7	PE860EC	Adaptive Signal Processing
8	PE880EC	Software Defined and Cognitive Radio networks

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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Project work / Internship

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week): 0:0:18	SEE Marks : 50	Course Code: **PW819EC**
Credits : 9	CIE Marks : 50	Duration of SEE : Viva-Voce

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. Selection of a suitable topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of project seminar report.

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.

Project seminar topics may be chosen by the student with advice and approval from the faculty members. Students are to be exposed to the following aspects of seminar presentation.

- Literature Survey
- Organization of the material
- Presentation of OHP slides / PC presentation
- Technical writing

Each student is required to:

1. Submit a one-page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through OHP, PC, Slide project followed by a 10 minutes discussion.
3. Submit a report on the seminar topic with list of references and slides used.

Project reviews are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

- Batch size shall be 2 (or) 3 students per batch.
- Project allocation by department.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Low Power VLSI Design

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE810EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To acquire knowledge of power dissipation in VLSI circuits. 2. Apply low power techniques in VLSI circuits.	On completion of the course, students will be able to 1 Understand the basics of VLSI technology. 2 Apply the physics of power dissipation. 3 Analyze the circuit techniques for dynamic power dissipation. 4 Apply the circuit techniques for leakage reduction. 5 Design low power arithmetic operators.

UNIT - I :

Physics of power dissipation in CMOSFET devices: introduction, Submicron MOSFET, Power dissipation in CMOS, short circuit dissipation , dynamic dissipation , load capacitance, Body Effect , Short Channel Effects , MOS Capacitances , Hot Carrier Effects.

UNIT - II :

CMOS Technology and Devices : Evolution of CMOS Technology, BiCMOS Technology, SOI CMOS Technology, Threshold Voltage , Narrow Channel Effects, Mobility & Drain Current, Subthreshold Current, Electron Temperature, Velocity Overshoot.

UNIT - III :

Circuits Techniques for Dynamic Power Reduction: Dynamic Power Consumption Components, Circuit Parallelization, Memory Parallelization, Voltage Scaling-Based Circuit Techniques: Multiple Voltages Techniques, Low Voltage Swing, Precomputation, Retiming, Gated Clocks, Circuit Technology-Dependent Power Reduction, Path Balancing.

UNIT - IV :

Circuit Techniques for Leakage Reduction: Leakage Components, Subthreshold Leakage Gate Leakage, Source/Substrate and Drain/Substrate P-N Junction Leakage, Circuit Techniques to Reduce Leakage in Logic, Dual Threshold CMOS, Multiple Supply Voltage, Runtime Standby Leakage Reduction Techniques, Leakage Control Using Transistor Stacks (Self-Reverse Bias), Sleep Transistor, Dynamic Vdd Scaling (DVS) • Dynamic Vth Scaling (DVTS).

UNIT - V :

Low-Power Arithmetic Operators : Introduction, Addition, 1-Bit Addition Cells, Sequential Adder, Propagate and Generate Mechanisms, Carry Select Adder, Carry Skip Adder, Logarithmic Number System, Logarithmic Adders, Power/Delay Comparison.

Learning Resources:

1. Low power cmos circuits technology, logic design and cad tools by Chtristian piguet.
2. Low power cmos vlsi circuit design by Koushik Roy & Sharath prasad.
3. Low-Voltage CMOS VLSI Circuits , James B. Kuo
4. https://onlinecourses.nptel.ac.in/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Global Positioning System

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE830EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To study basics of mathematics and science related to GNSS constellations 2 To understand the different coordinates for representation user position. 3 To study the different errors of GPS 4 To understand the GPS data formats for use of different applications 5 To acquire the knowledge of augmentation systems.	On completion of the course, students will be able to 1 Apply the knowledge of basic mathematics and science to understand the different GNSS constellations 2 Use of different coordinate systems used in user position estimation 3 Identifying the various errors of GPS. 4 Interpret the GPS data for different applications. 5 Importance of augmentation systems in various diversified applications.

UNIT - I :

GPS Fundamentals: . GPS Applications , GPS Constellation, Principle of operation, GPS Orbits, Orbital mechanics and satellite position determination, Time references, Geometric Dilution of Precision: Geometrical dilution of Precision, Veritical dilution of precision, Position dilution of precision.

UNIT - II :

Coordinate Systems and errors: Geometry of ellipsoid, geodetic reference system. Geoid, Ellipsoid, Global and Regional datum, World geodetic system- 84, Different coordinate systems, Various error sources in GPS: Satellite and receiver clock errors, Ephemeris error, Atmospheric errors, Receiver measurement noise and User Equavalent Range Error.

UNIT - III :

GPS measurements: GPS signal structure, C/A and P-codes, Code and carrier phase measurements, position estimation with pseudo range measurements, Spoofing and anti spoofing, GPS navigation and observation data formats.

UNIT - IV :

GPS Augmentation systems: Code-based and carrier based Differenetial GPS(DGPS) Techniques, DGPS errors, Wide area augmentation system-architecture, GAGAN, Local area augmentation system concept.

UNIT - V :

GPS Modernization and other satellite navigation systems: Future GPS satellites, New signals and their benefits, Hardware and Software improvements, GPS integration – GPS/Geo Information System, GPS/Inertial Navigation Systedm, GPS/pseudolite, GPS/cellular, GLONASS, Galileo System.

Learning Resources:

1 Pratap Misra and Per Enge, "Global Positioning System Signals, Measurement, and Performance," Ganga- Jamuna Press, 2/e, Massachusetts, 2010.
2 G.S.Rao, Global Navigation Satellite Systems, Tata Mc Graw-Hill, 2010.
3 Satheesh Gopi, "Global positioning system: Principles and Application", TMH, 2005.
4 B.Hofmann-Wellenhof, H.Lichtenegger, and J.Collins, "GPS Theory and Practice," Springer Verlog, 2008.
5 Bradford W.Parkinson and James J. Spilker, "Global Positioning System: Theory and Application," Vol.II, American Institution of Aeronautices and Astronautics Inc., Washington, 1996.
6 https://nptel.ac.in/syllabus/105107062/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	20
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Image and Video Processing Using Machine Learning

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE850EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To introduce students to the basic concepts and techniques of Machine Learning and become familiar with regression methods, classification methods, clustering methods.	On completion of the course, students will be able to 1 Gain knowledge about basic concepts of Machine Learning 2 Identify machine learning techniques suitable for a given problem 3 Solve the problems using various machine learning techniques 4 Appreciate the underlying mathematical relationships within and across Machine Learning algorithms and the paradigms of supervised and un-supervised learning. 5 Design and implement various machine learning algorithms in a range of real-world applications.

UNIT - I :

Introduction to Machine learning, Core concepts, Data inconsistencies, Practical Machine learning applications, Types of learning problems, Machine learning architecture, Machine learning algorithms.

Linear Regression, Cost Function, Gradient descent and Logistic Regression.

UNIT - II :

Working with Decision tress: Basics of Decision trees, uses, Advantages, Limitations, different algorithm types - ID3, C4.5, CART

Bayesian Networks: Graph theory, probability theory, Bayes theorem, working of Bayesian Networks, Node counts, using Domain Experts.

UNIT - III :

Support vector Machines: Definition of SVM, uses of SVM, Basic classification principles, How Support Vector Machines Approach classification, Clustering: Definition of clustering, clustering types-K-means, Agglomerative hierarchical, DBSCAN.

UNIT - IV :

Deep learning: Background, Deep learning Taxonomy, Convolutional Neural networks, Recurrent Neural Networks, Restricted Boltzmann Machine, Deep Boltzmann Machine,Autoencoders.

UNIT - V :

Applications of Machine learning: Image retrieval, Face recognition, Video classification. Image Segmentation using K-means clustering, Satellite Image Classification using Decision Trees.

Learning Resources:

1 Machine Learning for Big Data :Hands on for developers and technical professionals wiley publications, 2018 by Jason Bell.

2 Practical Machine Learning. Sunila Gollapudi, Packt publishers, 2016.

3 Introduction to Machine Learning, Ethem Alpaydin, third edition, PHI

4 https://nptel.ac.in/noc/individual_course.php?id=noc18-cs40

5 https://nptel.ac.in/courses/106106139/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Optical Networks

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE870EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To introduce students to the concepts of Optical Network design.	On completion of the course, students will be able to 1 Implement SONET for communication. 2 CO2: Contribute in the areas of optical network and WDM network design. 3 CO3: Implement simple optical network and understand further technology developments for future enhanced network. 4 CO4: Contribute in the area of network survivability. 5 CO5: Design WDM Network

UNIT - I :
SONET/SDH: optical transport network, IP, routing and forwarding, multiprotocol label switching.

UNIT - II :
WDM network elements: optical line terminals and amplifiers, optical add/drop multiplexers, OADM architectures, reconfigurable OADM, optical cross connects.

UNIT - III :
Control and management: network management functions, optical layer services and interfacing, performance and fault management, configuration management, optical safety.

UNIT - IV :
Network Survivability: protection in SONET/SDH & client layer, optical layer protection Schemes.

UNIT - V :

WDM network design: LTD and RWA problems, dimensioning wavelength routing networks, statistical dimensioning models. Access networks: Optical time division multiplexing, synchronization, header processing, buffering, burst switching, test beds, Introduction to PON, GPON, AON.

Learning Resources:

1 Rajiv Ramaswami, Sivarajan, Sasaki, "Optical Networks: A Practical Perspective", MK, Elsevier, 3rd edition, 2010.
2 C. Siva Ram Murthy and Mohan Gurusamy, "WDM Optical Networks: Concepts Design,and Algorithms", PHI, EEE, 2001

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Real Time Systems

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE820EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To Familiarize students with the aspects of developing a Real Time System and Policies for I/O management, memory management and fault tolerance in Real Time Operating Systems.	On completion of the course, students will be able to 1 Enumerate the need and the challenges in the design of hard and soft real time systems. 2 Compare different scheduling algorithms and the schedulability criteria. 3 Determine schedulability of a set of periodic tasks when sharing resources without getting deadlock. 4 Compare different commercial RTOS and can choose specific type for particular application. 5 To analyze evaluation techniques and reliability models for Hardware Redundancy

UNIT - I : Real Time System Characteristics

Introduction to RTS, Types of RTS, Task Types, Jobs – Periodic, Sporadic, Aperiodic, Applications of RTS, Predictability, Reference Model, Types of schedulers, Cyclic and Priority based Schedulers

UNIT - II : Real Time Schedulers

Cyclic, priority based schedulers – static/dynamic – RM, EDF, LST, Optimality of EDF, Non-optimality of EDF, Scheduling with precedence constraints, Multiprocessor scheduling – static and dynamic systems, Problems of Predictability in multi-processor systems, Predictability of preemptive priority based scheduling in uniprocessor systems, Performance Measure of validation techniques.

UNIT - III : Resource sharing and Deadlock avoidance

Resource Control, Model, Priority Inversion, Uncontrolled Priority Inversion, Blocking Time, Disadvantages of Priority inversion , Priority Inheritance Protocol, Deadlocks due to Priority Inheritance Protocol, Priority Ceiling Protocol, Deadlock Avoidance, Analysis of Priority Ceiling Protocol, Blocking time, context switches, Stack Sharing Priority Ceiling Protocol, example, Priority Ceiling Protocol in Dynamic Priority Systems, Preemption Levels, Fixed Preemption Level Systems like EDF, Basic Preemption Ceiling Protocol, Multiple units of resources, Priority ceiling, Preemption ceiling and stack based preemption ceiling protocols for multiple unit resources

UNIT - IV : Commercial RTOS

Unix and Windows as RTOS, Real –time POSIX, Different Types of commercial RTOS , features of VxWorks , µCOS and RTLINUX. Memory, I/O management policies and Interrupt handling in Different RTOS.
Comparison and study of RTOS: Vxworks and µCOS

UNIT - V : Fault-Tolerance Techniques & RTOS Application Domains

What causes failures, Fault types, Fault detection, Hardware and software Redundancy.
Case studies: RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Learning Resources:

1 uC/OS-III: The Real-Time Kernel and the Freescale Kinetis ARM Cortex-M4 Hardcover, 2011, Micrium, ISBN-13: 978-0982337523.
2 Jane W S Liu, “Real Time Systems” 2018 edition, Pearson, India.
3 David E. Simon “An Embedded Software Primer” Addison-Wesley publisher, 2004, ISBN 020161569X.
4 https://nptel.ac.in/courses/106105036/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	20
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Radar and Navigation Systems

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE840EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Derive and understand the Radar range equation and the parameters that depends on 2 Analyze the working of Various Radars 3 Understand the different Navigation methods	On completion of the course, students will be able to 1 Derive and discuss Radar range equation and nature of detection 2 Describe about CW Radar and MTI radar 3 Interpret different tracking radars 4 Explain principles of navigation, in addition to approach and landing aids as related to navigation 5 Describe about the navigation systems using the satellite

UNIT - I :

Introduction to radar, radar block diagram and operation, radar frequencies, Applications of radar, Prediction of range performance, minimum detectable signal, receiver noise, probability density function, SNR, Integration of radar pulses, radar cross-section of targets, PRF and range ambiguities, transmitter power, system losses.

UNIT - II :

Doppler effect, CW radar, FM CW radar, multiple frequency CW radar. MTI radar, delay line canceller, range gated MTI radar, blind speeds, staggered PRF, limitations to the performance of MTI radar, non-coherent MTI radar.

UNIT - III :

Tracking radar: sequential lobing, conical scan, monopulse: amplitude comparison and phase comparison methods, Radar antennas. Radar displays. Duplexer.

UNIT - IV :

Introduction - Four methods of Navigation. **Direction Finding -** The Loop Antenna – Loop Input Circuits – An Aural Null Direction Finder – The Goniometer – Errors in Direction Finding – Adcock Direction Finders – Direction Finding at Very High Frequencies – The LF/MF Four course Radio Range – VHF Omni Directional Range(VOR)

UNIT - V :

Recent Developments in Navigation systems: Hyperbolic Systems of Navigation (Loran and Decca) – Loran-A – Loran-C – The Decca Navigation System - The Omega System - GPS principle of operation, Position location determination, principle of GPS receiver and applications,

Learning Resource:

1. Merrill I. Skolnik ," Introduction to Radar Systems", 3rd Edition Tata Mc Graw-Hill 2003.
2. N.S.Nagaraja, "Elements of Electronic Navigation Systems", 2nd Edition, TMH, 2000.
3. Peyton Z. Peebles:, "Radar Principles", John Wiley, 2004 2. J.C Toomay, " Principles of Radar", 2nd Edition –PHI, 2004
4. Radar Systems and Radio Aids to Navigation, Sen & Bhattacharya, Khanna publishers
5. NPTEL Links: https://nptel.ac.in/courses/101108056/3

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Duration of Internal Tests: 60 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Adaptive Signal Processing

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE860EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To introduce some practical aspects of signal processing, and in particular adaptive systems 2 The basic principles of adaptation which cover various adaptive signal processing algorithms (e.g., the LMS algorithm,RLS algorithm) and its applications, such as adaptive noise cancellation, interference cancelling, system identification	On completion of the course, students will be able to 1 Design and apply optimal minimum mean square estimators and in particular linear estimators. 2 Implement and analyze Wiener filters and evaluate their performance. 3 Implement and apply LMS, RLS, and Kalman filters for given applications. 4 Estimate the innovation process for Kalman filtering problem. 5 Analyze vector Kalman filters for target tracking

UNIT - I :

Approaches to the development of adaptive filter theory. Introduction to filtering, smoothing and prediction. Wiener filter theory, introduction; Error performance surface; Normal equation; Principle of orthogonality; Minimum mean squared error;

UNIT - II :

Gradient algorithms; Learning curves; LMS gradient algorithm; LMS stochastic gradient algorithms; convergence of LMS algorithms.

UNIT - III :

Applications of adaptive filter to adaptive noise cancelling, Echo cancellation in telephone circuits and adaptive beam forming

UNIT - IV :

Kalman Filter theory; Introduction; recursive minimum mean square estimation for scalar random variables; statement of the Kalman filtering problem: the innovations process; Estimation of state using the innovations process; Filtering examples

UNIT - V :

Vector Kalman filter formulation. Examples. Applications of Kalman filter to target tracking.

Learning Resource:

1 Simon Haykins, "Adaptive signal processing", PHI, 1986. 3rd EDITION
2 Sophoclas, J. Orphanidies, "Optimum signal processing an introduction", McMillan, 1985.
3 Bernard Widrow, "Adaptive signal processing", PHI,1986
4 Bozic. SM., Digital and kalman Filtering
5 https://nptel.ac.in/syllabus/117105026/

The break-up of CIE : Internal Tests + Assignments + Quizzes

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VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Software Defined & Cognitive Radio Networks

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PE880EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand basic architecture of software defined radio 2 To study signal processing devices and architectures 3 To describe spectrum sensing techniques of cognitive radio	On completion of the course, students will be able to 1 Gain knowledge on software defined radio and cognitive radio. 2 Describe about signal processing devices and architectures 3 Discuss on software and hardware architecture of Software Defined and Cognitive Radio. 4 Analyze spectrum sensing methods 5 Implement CR and SDR applications on to FPGA and ASICS.

UNIT - I :

Introduction to SDR: What is Software-Defined Radio, The Requirement for Software-Defined Radio, Legacy Systems, The Benefits of Multi-standard Terminals, Economies of Scale, Global Roaming, Service Upgrading, Adaptive Modulation and Coding, Operational Requirements, Key Requirements, Reconfiguration Mechanisms, Handset Model, New Base-Station and Network, Architectures, Separation of Digital and RF, Tower-Top Mounting, BTS Hoteling, Smart Antenna Systems, Smart Antenna System Architectures, Power Consumption Issues, Calibration Issues, Projects and Sources of Information on Software Defined Radio

UNIT - II :

Basic Architecture of a Software Defined Radio: Software Defined Radio Architectures, Ideal Software Defined Radio Architecture, Required Hardware Specifications, Digital Aspects of a Software Defined Radio, Digital Hardware, Alternative Digital Processing Options for BTS Applications, Alternative Digital Processing Options for Handset Applications, Current Technology Limitations, A/D Signal-to-Noise Ratio and Power Consumption, Derivation of Minimum Power Consumption, Power Consumption Examples, ADC Performance Trends, Impact of Superconducting Technologies on Future SDR Systems.

UNIT - III :

Signal Processing Devices and Architectures: General Purpose Processors, Digital Signal Processors, Field Programmable Gate Arrays, Specialized Processing Units, Tilera Tile Processor, Application-Specific Integrated Circuits, Hybrid Solutions, Choosing a DSP Solution. GPP-Based SDR, Non real time Radios, High-Throughput GPP-Based SDR, FPGA-Based SDR, Separate Configurations, Multi-Waveform Configuration, Partial Reconfiguration, Host Interface, Memory-Mapped Interface to Hardware, Packet Interface, Architecture for FPGA- Based SDR, Configuration, Data Flow, Advanced Bus Architectures, Parallelizing for Higher Throughput, Hybrid and Multi-FPGA Architectures, Hardware Acceleration, Software Considerations, Multiple HA and Resource Sharing, Multi-Channel SDR.

UNIT - IV :

Cognitive Radio : Techniques and signal processing History and background, Communication policy and Spectrum Management, Cognitive radio cycle, Cognitive radio architecture, SDR architecture for cognitive radio, Spectrum sensing Single node sensing: energy detection, cyclostationary and wavelet based sensing-problem formulation and performance analysis based on probability of detection Vs SNR. Cooperative sensing: different fusion rules, wideband spectrum sensing-problem formulation and performance analysis based on probability of detection Vs SNR.

UNIT - V :

Cognitive Radio: Hardware and applications: Spectrum allocation models. Spectrum handoff, Cognitive radio performance analysis. Hardware platforms for Cognitive radio (USRP, WARP), details of USRP board, Applications of Cognitive radio

Learning Resource:

1 "RF and Baseband Techniques for Software Defined Radio" Peter B. Kenington, ARTECH HOUSE, INC, 2005.
2 "Implementing Software Defined Radio", Eugene Grayver, Springer, New York Heidelberg Dordrecht London, ISBN 978-1-4419-9332-8 (eBook) 2013.
3 "Cognitive Radio Technology", by Bruce A. Fette, Elsevier, ISBN 10:0-7506-7952-2, 2006.
4 "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", Hüseyin Arslan, Springer, ISBN 978-1-4020-5541-6 (HB), 2007

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Duration of Internal Tests: 60 Minutes

Professional Electives (R-17) (Students can opt for all professional electives from single stream or several streams)						
Professional Elective Stream	**Semester – VII**				**Semester – VIII**	
	Professional Elective – I	**Professional Elective – II**	**Professional Elective – III**	**Professional Elective – IV**	**Professional Elective – V**	**Professional Elective – VI**
Embedded Systems and VLSI Stream	IoT Architectures and protocols (PE710EC)	Advanced Embedded Systems (PE720EC)	Field Programmable Gate Arrays (FPGA) Architectures (PE730EC)	Electronic Instrumentation (PE740EC)	Low Power VLSI Design (PE810EC)	Real Time Systems (PE820EC)
Communication Engineering Stream	Mobile Cellular Communication (PE750EC)	Optical Fiber Communication (PE760EC)	Coding theory and Techniques (PE770EC)	Satellite communication (PE780EC)	Global Positioning System (PE830EC)	Radar and Navigation Systems (PE840EC)
Signal Processing Stream	DSP Processors and Architectures (PE790EC)	Speech and Audio Signal Processing (PE711EC)	Digital Image and Video Processing (PE721EC)	Biomedical Signal Processing (PE731EC)	Image and Video processing using Machine Learning (PE850EC)	Adaptive Signal Processing (PE860EC)
Networking Stream	Wireless Sensor Networks (PE741EC)	Network Security (PE751EC)	Network Management (PE761EC)	Voice and Data Networks (PE771EC)	Optical Networks (PE870EC)	Software Defined and Cognitive Radio networks (PE880EC)