VASAVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

ACCREDITED BY NAAC WITH 'A++' GRADE
Ibrahimbagh, Hyderabad-31
Approved by A.I.C.T.E., New Delhi and
Affiliated to Osmania University, Hyderabad-07

Sponsored
by
VASAVI ACADEMY OF EDUCATION
Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR
B.E. (ECE) VII and VIII Semesters
With effect from 2023-24
(For the batch admitted in 2020-21)
(R-20)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Phones: +91-40-23146040, 23146041
Fax: +91-40-23146090

Institute Vision

Striving for a symbiosis of technological excellence and human values

Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering and fostering ethical values

Department Mission

To inculcate a spirit of scientific temper and analytical thinking and train the students in contemporary technologies in Electronics and Communication Engineering to meet the needs of the industry and society with ethical values

B.E (ECE) Program Educational Objectives (PEO's)	
PEO I	Graduates will be able to identify, analyze and solve engineering problems.
PEO II	Graduates will be able to succeed in their careers, higher education, and research.
PEO III	Graduates will be able to excel individually and in multidisciplinary teams to solve industry and societal problems.
PEO IV	Graduates will be able to exhibit leadership qualities and lifelong learning skills with ethical values.

B.E. (ECE) PROGRAM OUTCOMES (PO's) Engineering Graduates will be able to:	
PO1	Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO2	Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO3	Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal and environmental considerations.
PO4	Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
PO11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Lifelong learning: Recognize the need, and for have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

B.E (ECE) PROGRAM SPECIFIC OUTCOMES (PSO's)	
PSO I	ECE students will be able to analyze and offer circuit and system level solutions for complex electronics engineering problems, keeping in mind the latest technological trends.
PSO II	ECE students will be able to apply the acquired knowledge and skills in modeling and simulation of communication systems.
PSO III	ECE students will be able to implement signal and image processing techniques for real time applications.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION **(R-20)** :: B.E. - ECE : SEVENTH SEMESTER (2023 - 24)

B.E (ECE) VII - SEMESTER								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits
		Hours per Week			Duration in Hrs	Maximum Marks		
		L	T	P/D		SEE	CIE	
THEORY								
U20PC710EC	Microwave Engineering	3	-	-	3	60	40	3
U20PC720EC	VLSI Design	3	-	-	3	60	40	3
U20PE7XXEC	Professional Elective – II	3	-	-	3	60	40	3
U20PE7XXEC	Professional Elective – III	3	-	-	3	60	40	3
U20PE7XXEC	Professional Elective – IV	3	-	-	3	60	40	3
PRACTICALS								
U20PC711EC	Microwave Engineering Lab	-	-	2	3	50	30	1
U20PC721EC	VLSI Design Lab	-	-	2	3	50	30	1
U20PW719EC	Project Seminar	-	-	2	-	-	30	1
-	NPTEL Certification Course : 8 or 12 weeks duration	-	-	-	-	-	-	2
TOTAL		**15**	**-**	**6**		**400**	**290**	**20**
GRAND TOTAL		**21**				**690**		
Left over hours will be allocated for : CC								
Note: Every Student shall complete one NPTEL course certification of 8 weeks duration (equivalent to 2 credits weightage) by the end of VII-Semester.								

Professional Electives (R – 20) : Semester – VII		
Professional Elective – II		
1.	U20PE710EC	Advanced Embedded Systems
2.	U20PE720EC	Optical Fiber Communication
3.	U20PE730EC	Speech and Audio Signal Processing
4.	U20PE740EC	Network Security
Professional Elective – III		
5.	U20PE750EC	FPGA Architectures and Applications
6.	U20PE760EC	Coding theory and Techniques
7.	U20PE770EC	Digital Image and Video Processing
8.	U20PE780EC	Network Management
Professional Elective – IV		
9.	U20PE790EC	VLSI Physical Design
10.	U20PE711EC	Satellite Communication
11.	U20PE721EC	Biomedical Signal Processing
12	U20PE731EC	Voice and Data Networks

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Microwave Engineering

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PC710EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Analyze the field components of waveguides 2. Understand the characteristics of Microwave sources and components	On completion of the course, students will be able to 1. Anlayze the E and H fields components of parallel and rectangular waveguides. 2. Describe the characteristics and applications of circular waveguides and cavity resonators. 3. Analyze the scattering parameters of microwave components. 4. Demonstrate the characteristics of Microwave sources. 5. Describe the characteristics of microwave solid-state devices.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2	2										2	
CO2	3	3	2	2		2						2		2	
CO3	3	3		2		2								2	
CO4	2	2				2	2					2		2	
CO5	2	3				2	2							2	

UNIT-I :

Guided waves: Propagation of TE, TM and TEM waves between parallel planes. Velocity of propagation, wave impedance, attenuation in parallel plane guides.

UNIT-II:

Wave Guides: TE and TM waves in rectangular waveguides, Wave Impedance, Characteristic Impedance, Attenuation in wave guides. Introduction to Circular wave guides, Cavity resonators, resonant frequency, Applications of cavity resonators.

UNIT-III:
Microwave Circuits and Components: Concept of Microwave circuit, Normalized voltage and currents, Introduction to scattering parameters and their properties, Reciprocal and Non-reciprocal components: E and H Plane Tees, Magic Tee Directional coupler, Attenuators, Phase Shifters, Isolators and circulators S parameters for and their properties.

UNIT-IV:
Microwave Tubes: High frequency limitations of conventional tubes, Bunching and velocity modulation, mathematical theory of bunching, principles and operation of two cavity, multi cavity, Reflex Klystron. Principle and operation of magnetrons, TWT.

UNIT-V:
Microwave Solid State Devices: Principles of operation, characteristics and applications of Varactor, PIN diode, GUNN diode and IMPATT diode, Elements of strip lines of micro strip lines. Design analysis of microstrip lines.

Learning Resources:

1. Samuel Y. Liao, Microwave Devices and Circuits, 3rd ed, Pearson, 2003.
2. Edward C. Jordon, Keith G. Balmain, "Electromagnetic Waves and Radiating Systems", 2015, Pearson, 2nd Edition.
3. R.E. Collins, "Foundations of Microwave Engineering", II edition, Wiley, 2001.
4. K.C. Gupta "Microwaves", John Wiley & Sons, 2012
5. Annapurna Das, Sisir K. Das, "Microwave Engineering" Tata McGraw-Hill Education, 2000
6. https://swayam.gov.in/nd1_noc19_ee57
7. https://swayam.gov.in/nd1_noc19_ee68

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Design

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PC720EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the MOS fabrication technologies, electrical properties and develop layout of MOS circuits, subsystem, memory elements and perform testing.	On completion of the course, students will be able to 1 Acquire fundamental knowledge on MOSFET characteristics and its parameters 2 Analyze the fabrication process and physical design of CMOS circuits. 3 Identify the suitable basic digital building blocks in the design of digital systems. 4 Analyze the various types of memory cells. 5 Identify testing methods in VLSI Design.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	2		1								3		
CO2	2	2	1										1		
CO3	1	3		3									2		
CO4	1	3	3									2	3		
CO5	2	2		2	1							2	1		

UNIT-I:

Basic electrical properties of MOSFET: MOS Transistor threshold voltage, trans conductance, output conductance, Figure of merit, Body Effect, pull-up to pull-down ratio for NMOS inverter driven by another NMOS inverter/one or more pass transistors, NMOS transistor model, Sheet Resistance, Area Capacitance.

UNIT-II:

Introduction to CMOS fabrication process, Twin tub Process, latch up in CMOS circuits.

CMOS circuit physical design process: MOS Layers, Stick diagrams, Euler Path in stick diagram, Design rules, types of design rules, Layout diagrams of Basic CMOS Logic gates.

UNIT-III:
CMOS Subsystem design: Architectural issues, Carry select adder, carry save adder and Carry Skip adder, Multiplication: array multiplication, Wallace tree multiplication. Multiplexer and D Flip-Flop using Transmission gates.

UNIT-IV:
Design of Basic Memory Cells: Classifications of Memories, one and three transistor dynamic RAM cells, four transistor and six transistor Static RAM, Read only memory: Basic ROM architecture, NOR and NAND based ROM Memory Design. EPROM, EEPROM.

UNIT-V:
CMOS testing: role of testing, types of testing, functionality tests, manufacturing tests, stuck-at faults, short circuit and open circuit faults, controllability , observability, delay fault testing, level sensitive scan design, Boundary scan architecture.

Learning Resources:

1. Kamran Eshraghian, Douglas A. Pucknell, "Basic VLSI Design", PHI.
2. Introduction to VLSI circuits and Systems by John P. Uyemura, Wiley student edition.
3. Neil H.Weste, kamraneshraghan, "Principles of CMOS VLSI design", Pearson education.
4. https://nptel.ac.in/courses/108107129/
5. https://nptel.ac.in/courses/117101058/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Microwave Engineering Lab

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: **U20PC711EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Understand the basic characteristics of Microwave sources 2 Verify the relationship between guided wavelength and free space wavelength 3 Understand the measurement of various parameters of microwave components	On completion of the course, students will be able to 1 Describe the characteristics of microwave sources 2 Estimate the guide wave length and free space wave length 3 Measure the VSWR and impedance of unknown load 4 Determination of the scattering matrix of microwave Components/Junctions 5 Demonstrate characteristics of ferrite devices

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2		2		1	2							2	
CO2	3	3	2	2	3	2								2	
CO3	3	3		2										2	
CO4	3	3		2	2		2							2	
CO5	3			2										2	

Experiments:

1. Characteristics of Reflex Klystron oscillator
2. Characteristics of Gunn diode oscillator
3. Measurement of frequency and Guide wavelength
4. Measurement of VSWR of a given load
5. Measurement of impedance
6. Scattering matrix of a Directional coupler.
7. Scattering matrix of Waveguide Tees: E plane, H plane

8. Scattering matrix of Magic Tee.
9. Characteristics of Isolator and its scattering matrix
10. Characteristics of Circulator and its scattering matrix
11. Calibration of attenuator at a given frequency
12. Calibration of frequency meter at a given frequency

New / Additional experiments planned:

1. Design and analysis of Microstrip filter using ADS
2. Measurement of S-parameters using vector network analyser.

Mini Project(s):

Simulation and analysis of waveguide components

Learning Resources:

1. Advanced Design Software(ADS)

The break-up of CIE :

1. No. of Internal Tests	:	1
2. Max. Marks for internal tests	:	12
3. Marks for day-to-day laboratory class work	:	18

Duration of Internal Tests: 3 Hours

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VLSI Design Lab

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: **U20PC721EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To perform VLSI design of CMOS circuits using EDA Tools.	On completion of the course, students will be able to 1. Demonstrate the knowledge of digital circuit design flow. 2. Analyse the process of simulation of combinational sequential circuits. 3. Validate and demonstrate the results of digital circuits.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2		2		3								3		
CO2	1	2			2								1		
CO3	1	2	1		3								2		

1. Characteristics of NMOS and PMOS transistors.
2. Design and simulate CMOS inverter.
3. Design and simulate two input CMOS NAND/NOR gate.
4. Design and simulate CMOS Full adder
5. Design and simulate the D-Flip Flop.
6. Simulate the dynamic memory 1 Transistor and 3 Transistor cells.
7. Simulate the static memory 6 Transistor cell.
8. Layout of CMOS inverter
9. Perform DRC and LVS of CMOS inverter
10. Perform parasitic extraction of CMOS inverter
11. Perform Post layout level simulation of CMOS inverter
12. Perform CMOS circuit testing for stuck at 1 and stuck at o faults.

New / Additional experiments planned:

1. Design and simulate 4-bit carry select adder.
2. Simulate the static memory 4 transistor SRAM memory cell.

Note:

Minimum of twelve experiments are to be conducted.

The break-up of CIE : Internal Tests + Day to day Assignments

1.	No. of Internal Tests	:	1
2.	Max. Marks for internal tests	:	12
3.	Marks for day-to-day laboratory class work	:	18

Duration of Internal Test: 3 Hours

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Project Seminar

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 0:0:3	SEE Marks : -	Course Code: **U20PW719EC**
Credits : 1	CIE Marks : 30	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. To select the complex engineering problems beneficial to the society after thorough literature survey 2. To identify the modern tools for solving the problems. 3. To analyze and comprehend the experimental results 4. To communicate effectively the experimental results with report and presentation following ethics 5. To work in teams and adapt for the advanced technological changes

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3				2									
CO2		2			3										
CO3		2		3											
CO4								3		3					
CO5									3			3			

Note: CO1 & CO2 must be mapped with one of the relevant PSOs based on the domain of the project with 3
CO3: can be mapped to appropriate PSO with level 2

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.

Project seminar topics may be chosen by the student with advice and approval from the faculty members. Students are to be exposed to the following aspects of seminar presentation.

- Selection of Topic & Literature Survey (5M)
- Solution & Clarity in Implementation (5M)
- Modern Tool usage & Implementation (5M)
- Results and Analysis (5)
- Team Work / Report writing & Presentation with ethics (10M)

Each student is required to:

1. Submit a one-page synopsis in the beginning of the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through LCD power point presentation followed by a 10 minutes discussion.
3. Submit a report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

Students are required to submit a report on the project seminar.

- Batch size shall be 2 (or) 3 students per batch.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project seminar report.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Embedded Systems

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code : **U20PE710EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Define and classify embedded system and to interpret design process and challenges. 2 Summarize the RISC concepts and describe the ARM architecture, Interpret serial and parallel bus communication protocols. 3 Describe system design and co-design issues along with various laboratory, IDE tools and design case studies.	On completion of the course, students will be able to 1 Define embedded system & describe the embedded system product design life cycle and challenges. 2 Analyse the ARM Core embedded design and its programming model. 3 Apply knowledge to design networked embedded systems using serial, parallel and wireless communication protocols. 4 Justify the importance of hardware software co-design and models involved. 5 Acquire the knowledge of embedded IDEs to design and specify debugging techniques.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	2									1	3		
CO2	3	2	3	2	2				1			1	3	2	1
CO3	3	2	3	2	2				1			1	3	2	1
CO4	2	2	3	1	1				1			1	3	2	1
CO5	3	1	2									1	3		

UNIT – I :

Embedded System Design: Introduction, Trends, Definition, Classifications; Embedded Product Development Life Cycle. CPU selection– hardware, software, memories, and I/O. Challenges in designing Embedded System; Design Metric of Embedded System.

UNIT - II:

ARM Cortex-M based microcontroller architecture: ARM ISA, Interrupts and Processor Reset Sequence, Memory Address Map, ARM Registers, Nested VIC, AMBA Bus System and Bus Matrix, Memory and Peripherals, Debug System; Exceptions and Interrupts Architecture.

UNIT - III:

Embedded Networking: Traditional Networking Vs Embedded Networking; Networking through serial protocols: UART, I2C, SPI, CAN, IEEE1394 and USB; Porting of TCP/IP – Socket selection; HTTP client-server model; Design Considerations.

UNIT - IV:

Hardware Software Co-design: Comparison of Co-design Approaches; Formulation of the HW/SW scheduling, Optimization of Design Metric: Case study of Embedded Adaptive Cruise Control Design.

Embedded Software Architectures: Round Robin, RR with Interrupt driven and Functional Queue architectures.

UNIT - V:

Embedded Development tools: Host and Target machines, Instruction packing: Big-endian ISA Vs Little Endian ISA; Intel Vs Motorola Modes.

Debugging Methods: Testing on Host–Instruction set Simulators, native tools–IDEs; cross-compilers; ICE, JTAG, laboratory tools: Multi meter, CRO, Logic Analyzer & protocol sniffers.

Learning Resource:

1 Mohammed Tahir and Kashif Javed "ARM® Microprocessor Systems Cortex®-M Architecture, Programming, and Interfacing" CRC Press, 2017

2 Tony Givargis Frank Vahid "Embedded System Design: A Unified Hardware/Software Introduction" Wiley Student Edition, 2006

3 MOOCs: https://nptel.ac.in/noc/individual_course.php?id=noc19-cs22

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Optical Fiber Communication

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE720EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize with the optical sources, detectors and optical communication links.	On completion of the course, students will be able to 1 Describe the principles fiber-optic communication, the components and the bandwidth advantages. 2 Apply the properties of the optical fibers and optical components. 3 Use optical sources and detectors for various applications. 4 Analyze system performance of optical communication systems. 5 Design optical networks and understand non-linear effects in optical fibers.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3											1	2	
CO2	2	2	2	2										3	
CO3	1	2											2	3	
CO4	2	3										2		2	
CO5	2	2										2		2	

UNIT – I:

Introduction to vector nature of light, propagation of light, propagation of light in a cylindrical dielectric rod, Ray model, wave model.

UNIT - II:

Different types of optical fibers, Modal analysis of a step index fiber.
Signal degradation on optical fiber due to dispersion and attenuation. Fabrication of fibers and measurement techniques like OTDR.

UNIT - III:

Optical sources - LEDs and Lasers, Photo-detectors - pin-diodes, APDs, detector responsivity, noise, optical receivers. Optical link design - BER calculation, quantum limit, power penalties.

UNIT - IV:

Optical switches - coupled mode analysis of directional couplers, electro-optic switches. Optical amplifiers - EDFA, Raman amplifier. WDM and DWDM systems. Principles of WDM networks

UNIT - V:

Nonlinear effects in fiber optic links. Concept of self-phase modulation, group velocity dispersion and solition based communication.

Learning Resources:

1 J. Keiser, Fibre Optic communication, McGraw-Hill, 5th Ed. 2013 (Indian Edition).
2 G. Agrawal, Fiber optic Communication Systems, John Wiley and sons, 3rd Ed, 2002.
3 K.C. Gupta, Opto Electronic Devices and Systems, PHI Learning, 2005.
4 https://nptel.ac.in/courses/117101054/
5 https://nptel.ac.in/courses/117104127/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Speech and Audio Signal Processing

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE730EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the mechanism of speech production. 2 To analyze various speech synthesizers. 3 To study various types of coders and decoders. 4 To analyze speaker identification and verification systems.	On completion of the course, students will be able to 1 Apply the knowledge of science to design an artificial model of speech production system. 2 Analyse the types of speech signals & convert the signals to digital. 3 Synthesize the speech signal using a text as input. 4 Design speech encoder and decoder. 5 Also design an Automatic speech recognition system (ASR) by pattern matching method.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1	2			2					3	2			3
CO2	2	3	2								2	2			3
CO3	2	3	3			2					2	2			3
CO4	3	3	3								3	2			3
CO5	2	3	3							2	2	1			3

UNIT - I :

Applications of Digital Speech Processing, Phonetic Representation of Speech, Models for Speech Production-Schematic model of the vocal tract system, Source filter model for a speech signal production. Speech Quantization- Scalar quantization–uniform quantizer, optimum quantizer, logarithmic quantizer, adaptive quantizer, differential quantizers; Vector quantization.

UNIT - II :

Short-Time Analysis of Speech-Short-Time Energy and Zero-Crossing Rate, Short-Time Autocorrelation Function (STACF), Short-Time Fourier

Transform (STFT), The Speech Spectrogram, Relation of STFT to STACF. Pitch-period estimation Homomorphic Speech Analysis.

UNIT - III :

Speech Synthesis Methods, Linear predictive synthesizer, phone use synthesis, Introduction to Text-to-Speech and Articulator speech synthesis.

UNIT - IV :

Sub-band coding, Transforms coding, channel decoder, Formant decoder, Cepstral decoder, linear predictive decoder, vector quantizer coder.

UNIT - V :

Automatic Speech Recognition (ASR), The Problem of Automatic Speech Recognition, Building a Speech Recognition System, The Decision Processes in ASR, Representative Recognition Performance, Challenges in ASR Technology.

Learning Resources:

1. Lawrence R. Rabiner and Ronald W. Schafer, "Introduction to Digital Speech Processing", now, 2007.
2. Owens F.J., "Signal Processing of Speech", Macmillan, 2000.
3. Daniel Jurefskey & James H. Martin, "Speech and Language Processing", Pearson Education, 2003.
4. https://nptel.ac.in/courses/117105145/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Network Security

(Professional Elective-II)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE740EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To acquire knowledge on standard algorithms used to provide confidentiality, integrity and authenticity. 2 To understand the various key distribution and management schemes and to deploy encryption techniques to secure data in transit across data networks.	On completion of the course, students will be able to 1 Analyze the vulnerabilities in any computing system and able to design a security solution 2 Identify the security issues in the network and resolve it. 3 Evaluate security mechanisms using rigorous approaches 4 Analyze network security and web security requirements. 5 Illustrate the applications in networksecurity

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												2	
CO2	3	2												2	
CO3	3	2												2	
CO4	2	2	2											2	
CO5	3	2												2	

UNIT - I :

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security, Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques. Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Block Cipher Design Principles.

UNIT - II :

Encryption: Triple DES, International Data Encryption algorithm, Characteristics of Advanced Symmetric block ciphers. Conventional Encryption Placement of Encryption function

UNIT - III :

Public Key Cryptography Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange , Number Theory in brief.

UNIT - IV :

Message Authentication and Hash Functions Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME

UNIT - V :

IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms: Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems

Learning Resources:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.
3. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
4. https://nptel.ac.in/courses/106105031/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FPGA Architectures and Applications

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE750EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize the students with the architectural aspects of FPGA's and testing technologies of FPG's.	On completion of the course, students will be able to 1. Differentiate between ROM, PAL, PLA, SPLD, CPLD, and FPGA. 2. Apply the working of building blocks of FPGA to compare area and power efficiency. 3. Compare the features of Various FPGAs in terms of their Architecture, Configurable logic block. 4. Gain knowledge on placement and routing algorithms adopted in FPGAs. 5. Test a particular PLD using various techniques like design validation, Timing verification.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2										3		
CO2	2	2	1										1		
CO3	2	2	1	1	1								1		
CO4	3	2	1										1		
CO5	1	1	1	1	1								2		

UNIT - I: Introduction to PLD's and PGA'S

Memory- Read-only memory, read/write memory - SRAM and DRAM. Programmable Logic Devices-PLAs, PALs and their applications; Sequential PLDs and their applications; State- machine design with sequential PLDs; Programmable gate arrays (pgas), Introduction to field programmable gate arrays (FPGAs),design flow using FPGA, programming technologies.

UNIT - II: FPGA Architectural Aspects

Field Programmable Gate Arrays: Organization of FPGAs, Programmable Logic Block Architectures, Programmable Interconnect, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs,

Applications of FPGAs
Logic Block Architectures: Logic block functionality versus area-efficiency, Logic block area and routing model, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT - III: FPGA Architectures and Comparison
FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, virtexII FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT - IV: Placement and Routing Algorithms in FPGA Architectures
Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT - V:Testing methods in FPGA Architectures
Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps. Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Learning Resources:

1. S. Brown, R. Francis, J. Rose, Z.Vransic, "Field Programmable Gate array", BSP, 2007.
2. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
3. Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010
4. S. Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
5. https://nptel.ac.in/syllabus/117108040/prof.Kuruvilla Varghese IISC Banglore

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Coding Theory and Techniques

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE760EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To study the source coding and channel coding techniques digital data storage and transmission.	On completion of the course, students will be able to 1 Apply the probabilistic method to construct different types of source codes. 2 Identify different types of errors and to comprehend various linear block codes 3 Construct convolution codes for error detection and correction. 4 Generate LDPC codes using different methods of constructions 5 Construct Galois Fields and to apply them to generate BCH and RS codes

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2											2	
CO2	3	3	2											3	
CO3	3	2	2											3	
CO4	3	2												3	
CO5	3	2	2											3	

UNIT - I:

Coding for Reliable Digital Transmission and Storage: Source coding: Entropy encoding algorithms: Arithmetic coding and Golomb coding, Dictionary codes: Lempel-Ziv codes, Run Length Encoding.

UNIT - II:

Linear Block codes: Introduction to Linear Block Codes, Hamming codes, Repetition codes, Reed-Muller codes, the (24,12) Golay code, Product codes, Interleaved codes.

UNIT - III:

Convolutional codes: Encoding, Structural properties, State diagram, Code tree diagram, soft decision and hard decision decoding, Viterbi algorithm.

UNIT - IV:

Low Density Parity Check codes: Introduction, Properties, Graphical Representation of LDPC Codes: Tanner graphs, Types of constructions, Regular and Irregular LDPC codes, methods of constructing LDPC codes: Galleger's method, Alzebraic method, Mackay construction, Encoding and problems.

UNIT - V:

BCH and RS codes: Groups, Fields, Binary arithmetic, Construction of Galois Fields GF(2^m), Basic properties of Galois Fields, Introduction to BCH and RS codes (Encoding only).

Learning Resource:

1. K. Deergha Rao, 'Channel Coding Techniques for Wireless Communications," Second Edition, Springer 2019
2. Shu Lin and Daniel J. Costello, Jr. "Error Control Coding," 2/e, Pearson, 2011.
3. K Sam Shanmugum, "Digital and Analod Communication Systems," Wiley,2010.
4. Simon Haykin, "Digital Communication," TMH, 2009.
5. https://nptel.ac.in/courses/117106031/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Digital Image and Video Processing

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE770EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will gain knowledge on digital image and video processing techniques.	On completion of the course, students will be able to 1 Describe the basic concepts of Image and Video Processing 2 Apply the equations to transform images into different domains. 3 Apply spatial and transform domain techniques to process images. 4 Analyse quality of processed images using appropriate metrics 5 Design and implement various image and video processing techniques in a range of real-world applications.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2													2
CO2	2	3			2										3
CO3	2	3			2										3
CO4	2	3		2	2										3
CO5	2	3	3	3	2										3

UNIT - I:

Digital Image Fundamentals-Elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels – neighbourhood, adjacency, connectivity, distance measures.

UNIT - II:

Fourier transform, FFT, Discrete cosine transform, Hadamard transform, Slant transform and their properties.
Wavelet Transforms: Discrete Wavelet Transforms.

UNIT - III:

Spatial enhancement techniques: Basic Intensity Transformation functions, Histogram equalization, Histogram specification, Spatial Filtering Techniques.

Frequency domain techniques: Low pass, High pass and Homomorphic Filtering.

Image Degradation model, Algebraic approach to restoration, inverse filtering, Least mean square filter.

Quality assessment of enhanced images.

UNIT - IV:

Image Compression-Redundancy–inter-pixel and psycho-visual, Huffman Coding, Arithmetic coding, Lossless compression – predictive, Lossy compression-predictive and Transform coding techniques (JPEG and JPEG2000).

Image Segmentation - Point, Line and Edge Detection, thresholding - global, region-based segmentation.

Quality assessment of compressed / restored and segmented images.

UNIT - V:

Video formation, perception, and representation, two-dimensional motion estimation.

Fingerprint image enhancement, Compression of Satellite images using JPEG, Medical image segmentation, Object tracking in videos.

Learning Resources:

1 R.C. Gonzalez and R.E. Woods, Digital Image Processing, 4th Edition, Pearson, 2018.
2 Anil Kumar Jain, Fundamentals of Digital Image Processing, Prentice Hall of India. 2nd edition 2004.
3 Video Processing and Communications Yao Wang, Jorn stermann, and Ya-Qin Zhang Prentice Hall, 2002 (Published September 2001).
4 Murat Tekalp, Digital Video Processing" Prentice Hall, 2nd edition 2015.
5 https://nptel.ac.in/courses/117/105/117105135/
6 https://nptel.ac.in/courses/117/105/117105079/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Network Management

(Professional Elective-III)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE780EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To familiarize the students with the network architectures and management issues.	On completion of the course, students will be able to 1. Explain network management perspectives 2. Apply various network management protocol 3. Identify and describe TMN standards 4. Analyze various management issues 5. Demonstrate how to correctly maintain LAN

UNIT - I:

Overview of Data Communication and Network Management – Goals, Organization and Functions; Network Management – Architecture and Organization; Network Management Perpestives; Current Status and Future of Network Management. Network Topology, Network Node Components, Transmission Technology.

UNIT - II:

Network Management Standards, Network Management Models, Organizational Model, Information Model, Communication Model. **SNMPv1 –**History of SNMP, Internet Organization and Standards, SNMP Model, Organizational Model, System Overview, Information Model. SNMP Communication Model, Functional Model.SNMPv2 and SNMv3.

UNIT - III:

TMN Conceptual Model, TMN Standards, TMN Architecture, TMN Management Service Architecture, TMN Integrated View, TMN Implementation.

UNIT - IV:

Configuration Management, Fault Management, Performance Management, Security Management, Service Level Management, Accounting Management, Report Management, Policy-Based Management.

UNIT - V:

Setting-UP LAN Access, SNMP configuration, Switched Port Analyzer, Web Browser / Web Server Communication. IP Network Management - Configuration, Management Information Base, Simple Network Management Protocol, IP-Based Service Implementation- Network Management Issues, OSS Architecture.

Learning Resources:

1. Mani Subramanian "Network Management - Principles and Practice", Addison-Wesley, 2000.
2. Salah Aiidarons, Thomas Plevayk, "Telecommunications Network Technologies and Implementations", Eastern Economy Edition IEEE press, New Delhi, 1998.
3. Lakshmi. G, Raman, "Fundamentals of Telecommunication Network Management", Eastern Economy Edition IEEE Press, New Delhi
4. J. Richard Burke, "Network Management: Concepts and Practice, A Hands-on Approach", Pearson Education, 2008.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Physical Design

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE790EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To draw Layout and stick diagrams of circuits and acquire the knowledge on cell based designs.	On completion of the course, students will be able to 1. Draw the structures of the components of VLSI design. 2. Apply the basic concepts of physical design to layouts and stick diagrams. 3. Analyze the process variations, fabrication errors and their effect on design rules 4. Analyze hierarchical circuit Layouts using cell concepts. 5. Illustrate the basic algorithms which are used in physical design automation.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2											3		
CO2	2	3	2										3		
CO3	3	2											3		
CO4	2	3	2										3		
CO5	3	2											3		

UNIT - I:

VLSI Design cycles and new trends in Design cycles, physical design cycles and new trends in physical design cycles, Components of VLSI, Various layers of VLSI, Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors

UNIT - II:

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects), physical design of logic gates – NOT, NAND and NOR. Mask overlays for different structures. Parasitics – latch up and its prevention

UNIT - III:

Device matching and common centroid techniques for analog circuits. Design rules – fabrication errors, alignment sequence, alignment inaccuracies and process variations, Scalable CMOS (SCMOS) design rules.

UNIT - IV:

Layout design,stick diagrams and Hierarchical stick diagrams.
Cell concepts – cell based layout design – Wein-berger image array — design hierarchies.

UNIT - V:

System level physical design- large scale physical design , interconnect delay modeling, cross talk, floor planning, routing and clock distribution.
Factors, Complexity Issues and NP-hard Problems, Basic Algorithms : Basic terminology, graph search algorithms

Learning Resources:

1. Algorithms for VLSI Physical Design automation, Naveed Sherwani.3rd edition Kluwer academic publishers
2. Algorithms for VLSI Design automation, SabithH. Gerez, John Wiley & sons, Inc.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
4. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
5. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.
6. https://nptel.ac.in/courses/106105161

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Satellite Communication

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE711EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the working principles of various satellites and their importance in global communication 2 To acquire the knowledge on satellite sub systems and various factors affecting the function of communication satellite. 3 To study the need of multiple access techniques and various protocols being used in satellite communications	On completion of the course, students will be able to 1 Apply Kepler's law to find satellite orbital paramters. 2 Describe satellite subsystems like telemetry, tracking and command control. 3 Analyze Satellite link design 4 Describe the various multiple access techniques. 5 Understand the importance of special purpose communication satellite and their applications.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3		1		1								2	
CO2	3	3		1		2								2	
CO3	3	2		2		2								2	
CO4	3	2		2		2								2	
CO5	3	3		1		2								2	

UNIT – I

Evolution and growth of communication satellites, synchronous satellites, frequency allocation, orbits, orbital mechanism and kepler's laws, effects of orbital inclination, azimuth and elevation, range and angle, eclipse, placements of a satellite in geo-stationery orbit.

UNIT – II

Space segment, stabilization, communication sub systems, Telemetry, tracking and command, Attitude & orbital Control Systems, Power Systems, Earth segment, large and small Earth station antennas, Redundancy configuration, Thermal System.

UNIT - III

System noise temperature and G/T ratio, Basic RF link analysis, EIRP, C/N, Interference, attenuation due to rain, cross polarization, design of uplink and down link

UNIT - IV

Multiple access techniques, SCPC companding systems, TDMA frame structure, Frame efficiency, Super frame structure, frame acquisition and synchronization, types of demand assignments, SPADE.

UNIT - V

Special purpose communication satellites, INTELAST, Global Positioning System, Echo- Cancellation techniques, Protocols, Satellite applications, Introduction to NavIC system Indian activities in satellite communication.

Learning Resources:

1. Timothy Pratt and Charles W. Bostan, Satellite Communications, 2003.
2. Dr. D.C Agarwal, Satellite Communications 7th Edition, Khanna Publishers, 1996
3. Tri-T-ha, Digital Satellite Communications, 2nd Edition, McGraw Hill, 1990.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Biomedical Signal Processing

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE721EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To introduce the fundamentals of probability theory and random processes with biomedical signals applications. 2 To equip students with the fundamental tools that are used to describe, analyze and process biomedical signals. 3 To acquire the knowledge on fundamental principles in the analysis and design of filters, power spectral density estimation and non-stationary signal processing techniques with cardiological and neurological signals.	On completion of the course, students will be able to 1 Apply the probability theory and random processes techniques in analyzing biological signals. 2 Determine to best class of compression techniques to use for a particular bio medical signal to compress. 3 Possess the basic mathematical, scientific and computational skills necessary to analyze and process cardiological signals as per the requirement. 4 Ability to formulate and solve basic problems in biomedical signal analysis. 5 Possess the basic mathematical, scientific and computational skills necessary to analyze and process neurological signals as per the requirement.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2			2										3
CO2	3	2			2										3
CO3	3	2		2	2										3
CO4	3	2			2										3
CO5	3	2			2										3

UNIT – I

Discrete and continuous Random variables: Probability distribution and density functions. Gaussian and Rayleigh density functions, Correlation between random variables.

Stationary random process, Ergodicity, Power spectral density and autocorrelation function of random processes. Noise power spectral density analysis, Noise bandwidth, noise figure of systems.

UNIT – II

Data Compression Techniques: Lossy and Lossless data reduction Algorithms. ECG data compression using Turning point, AZTEC, CORTES, Huffman coding, vector quantisation, DCT and the K L transform.

UNIT – III

Cardiological Signal Processing: Pre-processing. QRS Detection Methods. Rhythm analysis. Arrhythmia Detection Algorithms. Automated ECG Analysis. ECG Pattern Recognition. Heart rate variability analysis.
Adaptive Noise Cancelling: Principles of Adaptive Noise Cancelling. Adaptive Noise Cancelling with the LMS Adaptation Algorithm. Noise Cancelling Method to Enhance ECG Monitoring. Fetal ECG Monitoring.

UNIT – IV

Signal Averaging, polishing – mean and trend removal, Prony's method, Prony's Method based on the Least Squares Estimate, Linear prediction. Yule – walker (Y –W) equations, Analysis of Evoked Potentials.

UNIT-V

Neurological Signal Processing: Modelling of EEG Signals. Detection of spikes and spindles Detection of Alpha, Beta and Gamma Waves. Auto Regressive (A.R.) modelling of seizure EEG. Sleep Stage analysis. Inverse Filtering. Least squares and polynomial modelling.

Learning Resources:

1. Probability, Random Variables & Random Signal Principles – Peyton Z. Peebles, 4th ed., 2009, TMH.
2. Biomedical Signal Processing- Principles and Techniques – D.C.Reddy, 2005, TMH.
3. Digital Bio signal Processing – Weitkunat R, 1991, Elsevier.
4. Biomedical Signal Processing – Akay M, IEEE Press.
5. Biomedical Signal Processing –Vol. I Time & Frequency Analysis – Cohen.A, 1986, CRC Press.
6. Biomedical digital Signal Processing: C-Language Experiments and Laboratory Experiments, Willis J.Tompkins, PHI.
7. https://nptel.ac.in/courses/108105101/ Biomedical Signal Processing – by Prof.Sudipta Mukhopadhyay. IITKGP
8. http://www.ecdept.iitkgp.ac.in/index.php/home/faculty/smukho

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Voice and Data Networks

(Professional Elective-IV)

SYLLABUS FOR B.E. VII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE731EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To acquire knowledge on concepts of voice communication, data communication and switching components in telecommunication systems.	On completion of the course, students will be able to 1 Design various types of networks considering their design conditions. 2 Apply various switching techniques. 3 Analyse various data networks and apply them using standard data link layer protocols 4 Apply standards of 3G and 4G. 5 Understand 5G technologies.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												2	
CO2	3	3												2	
CO3	3	3	2											2	
CO4	2	3												2	
CO5	3	3												2	

UNIT – I

Network requirements, Network Performance parameters, Network Terminology, Voice and data networks, Issues in design of voice and data networks. Network architecture, Network software.

UNIT – II

Switching, Three Stage Space Division Switch, Blocking and Non-blocking switching, Introduction to Signaling System Number 7 (SS7), Circuit Switching and Packet Switching, Multiplexing.

UNIT – III

Data Networks and their Design, Link layer design- Link adaptation, Link Layer Protocols. Hybrid ARQ (HARQ). Classless Inter domain Routing (CIDR), IP address lookup, Routing in Internet.

UNIT – IV

Evolution from 3G to 4G: 3G W-CDMA(UMTS), 3G CDMA, 3G TD-SCDMA, 3G evaluation to 4G, OFDM, LTE.

UNIT-V

Evolution of LTE technology to beyond 4G, 5G road map, Allocation of new spectrum for 5G, Spectrum sharing, 5G architecture, Overview of cognitive radio technology in 5G wireless, Spectrum optimization using cognitive radio.

Learning Resources:

1. L. Peterson and B. S. Davie, "Computer Networks: A Systems Approach", 5th Edition, Morgan Kaufman, 2011.
2. Theodore S. Rappaport, "Wireless Communications Principles and Practice" 2nd edition, Pearson, 2010.
3. Fundamentals of 5G Mobile Networks Hardcover, by Jonathan Rodriguez, Wiley.
4. 4G, LTE-Advanced Pro and The Road to 5G by Erik Dahlman.
5. D. Bertsekas and R. Gallager, "Data Networks", 2nd Edition, Prentice Hall, 1992.
6. Kumar, D. Manjunath and J. Kuri, "Communication Networking: An analytical approach", 1st Edition, Morgan Kaufman, 2004.
7. https://nptel.ac.in/courses/106105082

The break-up of CIE: Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) :: IBRAHIMBAGH, HYDERABAD – 500 031.
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION **(R-20)** :: B.E. – ECE : EIGHTH SEMESTER (2023 - 24)

B.E (ECE) VIII – SEMESTER								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits
		Hours per Week			Duration in Hrs	Maximum Marks		
		L	T	P/D		SEE	CIE	
THEORY								
U20PE8XXEC	Professional Elective – V	3	-	-	3	60	40	3
U20PE8XXEC	Professional Elective – VI	3	-	-	3	60	40	3
PRACTICALS								
U20PW819EC	Project / Internship	-	-	12	Viva-Voce	50	50	6
	TOTAL	**6**	**-**	**12**		**170**	**130**	**12**
	GRAND TOTAL	**18**				**300**		

Professional Electives (R – 20) : Semester – VIII		
Professional Elective – V		
1	U20PE810EC	Low Power VLSI Design
2	U20PE820EC	Global Positioning System
3	U20PE830EC	Image and Video processing using Machine Learning
4	U20PE840EC	Optical Networks
Professional Elective – VI		
5	U20PE850EC	Real Time Systems
6	U20PE860EC	Radar and Navigation Systems
7	U20PE870EC	Adaptive Signal Processing
8	U20PE880EC	Software Defined and Cognitive Radio networks

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Project work / Internship

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week): 0:0:12	SEE Marks : 50	Course Code: **U20PW819EC**
Credits : 6	CIE Marks : 50	Duration of SEE : Viva-Voce

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. To select the complex engineering problems beneficial to the society and develop solutions with appropriate considerations 2. To apply modern tools and analyze the results to provide valid conclusions. 3. To communicate effectively the solutions with report and presentation following ethics 4. To work in teams and adapt for the advanced technological changes 5. To apply management principles to complete the project economically

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3	3			2	2								
CO2				3	3										
CO3								3		3					
CO4									3			3			
CO5											3				

Note: CO1& CO2 must be mapped with one of the relevant PSOs based on the domain of the project with 3
CO4 can be mapped to appropriate PSO with level 2

Oral presentation is an important aspect of engineering education. The objective of the project is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.

Project topics may be chosen by the student with advice and approval from the faculty members. Students are to be exposed to the following aspects of project work carried out.

- Selection of topic & Literature survey (5M)
- Solution & Clarity in Implementation (5M)
- Modern tool usage in Implementation (10M)
- Results and Analysis (10M)
- Team Work, Report writing & Presentation with ethics (15M)
- Project Management (5M)

Each student is required to:

1. Submit a one-page synopsis in the beginning of project work for display on the notice board.
2. Give a 20 minutes presentation through LCD power point presentation followed by a 10 minutes discussion.
3. Submit a report on the project work with list of references and slides used.

Project reviews are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

- Batch size shall be 2 (or) 3 students per batch.
- Project allocation by department.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Low Power VLSI Design

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE810EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To acquire knowledge of power dissipation in VLSI circuits. 2. Apply low power techniques in VLSI circuits.	On completion of the course, students will be able to 1. Understand the basics of VLSI technology. 2. Apply the physics of power dissipation. 3. Analyze the circuit techniques for dynamic power dissipation. 4. Apply the circuit techniques for leakage reduction. 5. Design low power arithmetic operators.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2			2								2		
CO2	2	2	3										2		
CO3	2	2	2		2								2		
CO4		2	3		2								2		
CO5		2	2		2								2		

UNIT - I :

Physics of power dissipation in CMOSFET devices: introduction, Submicron MOSFET, Power dissipation in CMOS, short circuit dissipation, dynamic dissipation, load capacitance, Body Effect, Short Channel Effects, MOS Capacitances, Hot Carrier Effects.

UNIT - II :

CMOS Technology and Devices : Evolution of CMOS Technology, BiCMOS Technology, SOI CMOS Technology, Threshold Voltage , Narrow Channel Effects, Mobility & Drain Current, Subthreshold Current, Electron Temperature, Velocity Overshoot.

UNIT - III :

Circuits Techniques for Dynamic Power Reduction: Dynamic Power Consumption Components, Circuit Parallelization, Memory Parallelization, Voltage Scaling-Based Circuit Techniques: Multiple Voltages Techniques, Low Voltage Swing, Precomputation, Retiming, Gated Clocks, Circuit Technology-Dependent Power Reduction, Path Balancing.

UNIT - IV :

Circuit Techniques for Leakage Reduction: Leakage Components, Subthreshold Leakage Gate Leakage, Source/Substrate and Drain/Substrate P-N Junction Leakage, Circuit Techniques to Reduce Leakage in Logic, Dual Threshold CMOS, Multiple Supply Voltage, Runtime Standby Leakage Reduction Techniques, Leakage Control Using Transistor Stacks (Self-Reverse Bias), Sleep Transistor, Dynamic Vdd Scaling (DVS) • Dynamic Vth Scaling (DVTS).

UNIT - V :

Low-Power Arithmetic Operators : Introduction, Addition, 1-Bit Addition Cells, Sequential Adder, Propagate and Generate Mechanisms, Carry Select Adder, Carry Skip Adder, Logarithmic Number System, Logarithmic Adders, Power/Delay Comparison.

Learning Resources:

1. Low power CMOS circuits technology, logic design and cad tools by Chtristian piguet.
2. Low power CMOS VLSI circuit design by Koushik Roy & Sharath prasad.
3. Low-Voltage CMOS VLSI Circuits , James B. Kuo
4. https://onlinecourses.nptel.ac.in/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Global Positioning System

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE820EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To study basics of mathematics and science related to GNSS constellations 2 To understand the different coordinates for representation user position. 3 To study the different errors of GPS 4 To understand the GPS data formats for use of different applications 5 To acquire the knowledge of augmentation systems.	On completion of the course, students will be able to 1 Apply the knowledge of basic mathematics and science to understand the different GNSS constellations 2 Use of different coordinate systems used in user position estimation 3 Identifying the various errors of GPS. 4 Interpret the GPS data for different applications. 5 Importance of augmentation systems in various diversified applications.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2		2										2	
CO2	3	2		2										2	
CO3	3	2				2	2							2	
CO4	3					2	2					2		2	
CO5	3					2	2							2	

UNIT - I :

GPS Fundamentals: GPS Applications , GPS Constellation, Principle of operation, GPS Orbits, Orbital mechanics and satellite position determination, Time references, Geometric Dilution of Precision: Geometrical dilution of Precision, Veritical dilution of precision, Position dilution of precision.

UNIT - II :

Coordinate Systems and errors: Geometry of ellipsoid, geodetic reference system. Geoid, Ellipsoid, Global and Regional datum, World

geodetic system- 84, Different coordinate systems, Various error sources in GPS: Satellite and receiver clock errors, Ephemeris error, Atmospheric errors, Receiver measurement noise and User Equivalent Range Error.

UNIT - III :

GPS measurements: GPS signal structure, C/A and P-codes, Code and carrier phase measurements, position estimation with pseudo range measurements, Spoofing and anti spoofing, GPS navigation and observation data formats.

UNIT - IV :

GPS Augmentation systems: Code-based and carrier based Differential GPS(DGPS) Techniques, DGPS errors, Wide area augmentation system-architecture, GAGAN, Local area augmentation system concept.

UNIT - V :

GPS Modernization and other satellite navigation systems: Future GPS satellites, New signals and their benefits, Hardware and Software improvements, GPS integration – GPS/Geo Information System, GPS/Inertial Navigation Systedm, GPS/pseudolite, GPS/cellular, GLONASS, Galileo System.

Learning Resources:

1 Pratap Misra and Per Enge, "Global Positioning System Signals, Measurement, and Performance," Ganga- Jamuna Press, 2/e, Massachusetts, 2010.
2 G.S.Rao, Global Navigation Satellite Systems, Tata Mc Graw-Hill, 2010.
3 Satheesh Gopi, "Global positioning system: Principles and Application", TMH, 2005.
4 B. Hofmann-Wellenhof, H. Lichtenegger, and J. Collins, "GPS Theory and Practice," Springer Verlog, 2008.
5 Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Application," Vol. II, American Institution of Aeronautices and Astronautics Inc., Washington, 1996.
6 https://nptel.ac.in/syllabus/105107062/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Image and Video Processing Using Machine Learning

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE830EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To introduce students to the basic concepts and techniques of Machine Learning and become familiar with regression methods, classification methods, clustering methods.	On completion of the course, students will be able to 1 Describe the basic concepts of Machine Learning 2 Apply Machine Learning techniques suitable for a given problem. 3 Apply Deep Learning techniques suitable for a given problem. 4 Analyse the performance of various models using appropriate metrics. 5 Design and implement various machine learning algorithms in a range of real-world applications.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2													2
CO2	2	3			2										3
CO3	2	3			2										3
CO4	2	2		3	2										3
CO5	2	2	3	2	3										3

UNIT - I :

Introduction to Machine learning, Core concepts, Data inconsistencies, Practical Machine learning applications, Types of learning problems, Machine learning architecture, Machine learning algorithms.

Linear Regression, Cost Function, Gradient Descent and Logistic Regression.

UNIT - II :

Working with Decision tress: Basics of Decision trees, uses, Advantages, Limitations, different algorithm types - ID3, C4.5, CART

Bayesian Networks: Graph theory, probability theory, Bayes theorem, working of Bayesian Networks.

UNIT - III :

Support vector Machines: Definition of SVM, uses of SVM, Basic classification principles, How Support Vector Machines Approach classification.

Clustering: Definition of clustering, clustering types-K-means, Agglomerative hierarchical, DBSCAN.

UNIT - IV :

Deep learning: Background, Deep learning Taxonomy, Hebbian learning, Perceptron Learning, Back propagation, Convolutional Neural networks, Recurrent Neural Networks, Autoencoders.

UNIT - V :

Applications of Machine learning: Image retrieval, Face recognition, Video classification. Image Segmentation using K-means clustering, Satellite Image Classification using Decision Trees. Image/Video Classification using CNN, Performance analysis of various algorithms.

Learning Resources:

1 Machine Learning, Tom M. Mitchell, 1st Edition, McGraw-Hill Education; 1st edition, 2017.
2 Introduction to Machine Learning, Ethem Alpaydin, third edition, PHI.
3 Machine Learning for Big Data: Hands on for developers and technical professionals wiley publications, 2018 by Jason Bell.
4 Practical Machine Learning. Sunila Gollapudi, Packt publishers, 2016.
5 https://nptel.ac.in/courses/106/105/106105152/
6 https://nptel.ac.in/courses/106106139/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Optical Networks

(Professional Elective-V)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE840EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To introduce students to the concepts of Optical Network design.	On completion of the course, students will be able to 1 Implement SONET for communication. 2 CO2: Contribute in the areas of optical network and WDM network design. 3 CO3: Implement simple optical network and understand further technology developments for future enhanced network. 4 CO4: Contribute in the area of network survivability. 5 CO5: Design WDM Network

UNIT - I :
SONET/SDH: optical transport network, IP, routing and forwarding, multiprotocol label switching.

UNIT - II :
WDM network elements: optical line terminals and amplifiers, optical add/drop multiplexers, OADM architectures, reconfigurable OADM, optical cross connects.

UNIT - III :
Control and management: network management functions, optical layer services and interfacing, performance and fault management, configuration management, optical safety.

UNIT - IV :
Network Survivability: protection in SONET/SDH & client layer, optical layer protection Schemes.

UNIT - V :

WDM network design: LTD and RWA problems, dimensioning wavelength routing networks, statistical dimensioning models. Access networks: Optical time division multiplexing, synchronization, header processing, buffering, burst switching, test beds, Introduction to PON, GPON, AON.

Learning Resources:

1 Rajiv Ramaswami, Sivarajan, Sasaki, "Optical Networks: A Practical Perspective", MK, Elsevier, 3rd edition, 2010.
2 C. Siva Ram Murthy and Mohan Gurusamy, "WDM Optical Networks: Concepts Design,and Algorithms", PHI, EEE, 2001

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Real Time Systems

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE850EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To Familiarize students with the aspects of developing a Real Time System and Policies for I/O management, memory management and fault tolerance in Real Time Systems.	On completion of the course, students will be able to 1 Differentiate the design principles for hard and soft real time systems. 2 Compare different scheduling algorithms and the schedulability criteria for a real time system. 3 Determine schedulability of a set of periodic tasks when sharing resources avoiding dead lock. 4 Compare different commercial RTOS and choose specific type for a particular application. 5 To analyze evaluation techniques and reliability models for Hardware Redundancy

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1										1		
CO2	2	2	2												
CO3	2	2	2	1									1		
CO4	1	2	2	1											
CO5	1	1	3	1									2	2	2

UNIT - I : Real Time System Characteristics

Introduction to RTS, Types of RTS, Task Types, Jobs – Periodic, Sporadic, Aperiodic, Applications of RTS, Predictability, Reference Model, Types of schedulers, Cyclic and Priority based Schedulers and problem analysis.

UNIT - II : Real Time Schedulers

Cyclic, priority based schedulers – static/dynamic – RM, EDF, LST, Optimality of EDF, Non-optimality of EDF, Scheduling with precedence constraints, Multiprocessor scheduling – static and dynamic systems, Problems of Predictability in multi-processor systems, Preemptive and non-preemptive priority based scheduling in uniprocessor systems.

UNIT - III : Resource sharing and Deadlock avoidance

Resource Control Model, Priority Inversion, Uncontrolled Priority Inversion, Disadvantages of Priority inversion, Priority Inheritance Protocol, Deadlocks due to Priority Inheritance Protocol, Priority Ceiling Protocol, Deadlock Avoidance, Analysis of Priority Ceiling Protocol, Stack Sharing Priority Ceiling Protocol, Priority Ceiling Protocol in Dynamic Priority Systems, Multiple units of resources, Priority ceiling, Preemption ceiling and stack based preemption ceiling protocol.

UNIT - IV : Commercial RTOS

Unix and Windows as RTOS, Real-time POSIX, Different Types of commercial RTOS, features of VxWorks, µCOS and RTLINUX. Memory, I/O management policies and Interrupt handling in Different RTOS.
Comparison and study of RTOS: Vxworks and µCOS

UNIT - V: Fault-Tolerance Techniques & RTOS Application Domains

What causes failures, Fault types, Fault detection, Hardware and software Redundancy.
Case studies: RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Learning Resources:

1 uC/OS-III: The Real-Time Kernel and the Freescale Kinetis ARM Cortex-M4 Hardcover, 2011, Micrium, ISBN-13: 978-0982337523.
2 Jane W S Liu, "Real Time Systems" 2018 edition, Pearson, India.
3 David E. Simon "An Embedded Software Primer" Addison-Wesley publisher, 2004, ISBN 020161569X.
4 https://nptel.ac.in/courses/106105036/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Radar and Navigation Systems

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE860EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Derive and understand the Radar range equation and the parameters that depends on 2 Analyze the working of Various Radars 3 Understand the different Navigation methods	On completion of the course, students will be able to 1 Derive and discuss Radar range equation and nature of detection 2 Describe about CW Radar and MTI radar 3 Interpret different tracking radars 4 Explain principles of navigation, in addition to approach and landing aids as related to navigation 5 Describe about the navigation systems using the satellite

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3		2										2	
CO2	3	3		2		2								2	
CO3	3	3		2		2								2	
CO4	3	2		2		2	2							2	
CO5	3	2		2		2	2					2		2	

UNIT - I :

Introduction to radar, radar block diagram and operation, radar frequencies, Applications of radar, Prediction of range performance, minimum detectable signal, receiver noise, SNR, Integration of radar pulses, radar cross-section of targets, PRF and range ambiguities, transmitter power, system losses.

UNIT - II :

Doppler effect, CW radar, FM CW radar, multiple frequency CW radar. MTI radar, blind speeds, delay line cancellers, staggered PRF, limitations to the performance of MTI radar.

UNIT - III :

Tracking radars: Sequential lobing, Conical scan, Monopulse: amplitude comparison and phase comparison methods, Radar antennas. Radar displays. Duplexer.

UNIT - IV :

Direction Finding - Four methods of Navigation, Loop Antenna as direction finding, An Aural Null Direction Finder, Adcock Direction Finders, Direction Finding at Very High Frequencies: The LF/MF Four course Radio Range, VHF Omni Directional Range(VOR), Errors in Direction Finding.

UNIT - V :

Hyperbolic Navigation Systems: Principle of Hyperbolic Navigation Systems: Loran and Decca and Omega System, GPS principle and operation, Position location determination and applications.

Learning Resource:

1. Merrill I. Skolnik, "Introduction to Radar Systems", 2nd Edition Tata Mc Graw-Hill 2017.
2. N.S.Nagaraja, "Elements of Electronic Navigation Systems", 2nd Edition, TMH, 2000.
3. Peyton Z. Peebles:, "Radar Principles", John Wiley, 2004 2. J.C Toomay, "Principles of Radar", 2nd Edition –PHI, 2004.
4. Radar Systems and Radio Aids to Navigation, Sen & Bhattacharya, Khanna publishers
5. NPTEL Links: https://nptel.ac.in/courses/101108056/3

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Adaptive Signal Processing

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE870EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To introduce some practical aspects of signal processing, and in particular adaptive systems 2 The basic principles of adaptation which cover various adaptive signal processing algorithms (e.g., the LMS algorithm,RLS algorithm) and its applications, such as adaptive noise cancellation, interference cancelling, system identification	On completion of the course, students will be able to 1 Design and apply optimal minimum mean square estimators and in particular linear estimators. 2 Implement and analyze Wiener filters and evaluate their performance. 3 Implement and apply LMS, RLS, and Kalman filters for given applications. 4 Estimate the innovation process for Kalman filtering problem. 5 Analyze vector Kalman filters for target tracking

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1	2			2					3	2			3
CO2	2	3	2								2	2			3
CO3	2	3	3			2					2	2			3
CO4	3	3	3								3	2			3
CO5	2	3	3							2	2	1			3

UNIT - I :

Approaches to the development of adaptive filter theory. Introduction to filtering, smoothing and prediction. Wiener filter theory, introduction; Error performance surface; Normal equation; Principle of orthogonality; Minimum mean squared error;

UNIT - II :

Gradient algorithms; Learning curves; LMS gradient algorithm; LMS stochastic gradient algorithms; convergence of LMS algorithms.

UNIT - III :

Applications of adaptive filter to adaptive noise cancelling, Echo cancellation in telephone circuits and adaptive beam forming

UNIT - IV :

Kalman Filter theory; Introduction; recursive minimum mean square estimation for scalar random variables; statement of the Kalman filtering problem: the innovations process; Estimation of state using the innovations process; Filtering examples

UNIT - V :

Vector Kalman filter formulation. Examples. Applications of Kalman filter to target tracking.

Learning Resource:

1 Simon Haykins, "Adaptive signal processing", PHI, 1986. 3rd EDITION
2 Sophoclas, J. Orphanidies, "Optimum signal processing an introduction", McMillan, 1985.
3 Bernard Widrow, "Adaptive signal processing", PHI,1986
4 Bozic. SM., Digital and kalman Filtering
5 https://nptel.ac.in/syllabus/117105026/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Software Defined & Cognitive Radio Networks

(Professional Elective-VI)

SYLLABUS FOR B.E. VIII – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **U20PE880EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand basic architecture of software defined radio 2 To study signal processing devices and architectures 3 To describe spectrum sensing techniques of cognitive radio	On completion of the course, students will be able to 1 Gain knowledge on software defined radio and cognitive radio. 2 Describe about signal processing devices and architectures 3 Discuss on software and hardware architecture of Software Defined and Cognitive Radio. 4 Analyze spectrum sensing methods 5 Implement CR and SDR applications on to FPGA and ASICS.

UNIT - I :

Introduction to SDR: What is Software-Defined Radio, The Requirement for Software-Defined Radio, Legacy Systems, The Benefits of Multi-standard Terminals, Economies of Scale, Global Roaming, Service Upgrading, Adaptive Modulation and Coding, Operational Requirements, Key Requirements, Reconfiguration Mechanisms, Handset Model, New Base-Station and Network, Architectures, Separation of Digital and RF, Tower-Top Mounting, BTS Hoteling, Smart Antenna Systems, Smart Antenna System Architectures, Power Consumption Issues, Calibration Issues, Projects and Sources of Information on Software Defined Radio

UNIT - II :

Basic Architecture of a Software Defined Radio: Software Defined Radio Architectures, Ideal Software Defined Radio Architecture, Required Hardware Specifications, Digital Aspects of a Software Defined Radio, Digital Hardware, Alternative Digital Processing Options for BTS Applications, Alternative Digital Processing Options for Handset Applications, Current Technology Limitations, A/D Signal-to-Noise Ratio and Power Consumption, Derivation of Minimum Power Consumption, Power Consumption Examples, ADC Performance Trends, Impact of Superconducting Technologies on Future SDR Systems.

UNIT - III :

Signal Processing Devices and Architectures: General Purpose Processors, Digital Signal Processors, Field Programmable Gate Arrays, Specialized Processing Units, Tilera Tile Processor, Application-Specific Integrated Circuits, Hybrid Solutions, Choosing a DSP Solution. GPP-Based SDR, Non real time Radios, High-Throughput GPP-Based SDR, FPGA-Based SDR, Separate Configurations, Multi-Waveform Configuration, Partial Reconfiguration, Host Interface, Memory-Mapped Interface to Hardware, Packet Interface, Architecture for FPGA- Based SDR, Configuration, Data Flow, Advanced Bus Architectures, Parallelizing for Higher Throughput, Hybrid and Multi-FPGA Architectures, Hardware Acceleration, Software Considerations, Multiple HA and Resource Sharing, Multi-Channel SDR.

UNIT - IV :

Cognitive Radio : Techniques and signal processing History and background, Communication policy and Spectrum Management, Cognitive radio cycle, Cognitive radio architecture, SDR architecture for cognitive radio, Spectrum sensing Single node sensing: energy detection, cyclostationary and wavelet based sensing-problem formulation and performance analysis based on probability of detection Vs SNR. Cooperative sensing: different fusion rules, wideband spectrum sensing-problem formulation and performance analysis based on probability of detection Vs SNR.

UNIT - V :

Cognitive Radio: Hardware and applications: Spectrum allocation models. Spectrum handoff, Cognitive radio performance analysis. Hardware platforms for Cognitive radio (USRP, WARP), details of USRP board, Applications of Cognitive radio

Learning Resource:

1 "RF and Baseband Techniques for Software Defined Radio" Peter B. Kenington, ARTECH HOUSE, INC, 2005.
2 "Implementing Software Defined Radio", Eugene Grayver, Springer, New York Heidelberg Dordrecht London, ISBN 978-1-4419-9332-8 (eBook) 2013.
3 "Cognitive Radio Technology", by Bruce A. Fette, Elsevier, ISBN 10:0-7506-7952-2, 2006.
4 "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", Hüseyin Arslan, Springer, ISBN 978-1-4020-5541-6 (HB), 2007

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

Professional Electives (R-20)

(Students can opt for all professional electives from single stream or several streams)

Professional Elective Stream	Embedded Systems and VLSI Stream		Communication Engineering Stream		Signal Processing Stream		Networking Stream	
VI - Semester								
Professional Elective – I	U20PE610EC	IoT Architectures and protocols	U20PE620EC	Mobile Cellular Communication	U20PE630EC	DSP Processors and Architectures	U20PE640EC	Wireless Sensor Networks
VII - Semester								
Professional Elective – II	U20PE710EC	Advanced Embedded Systems	U20PE720EC	Optical Fiber Communication	U20PE730EC	Speech and Audio Signal Processing	U20PE740EC	Network Security
Professional Elective – III	U20PE750EC	FPGA Architectures and Applications	U20PE760EC	Coding theory and Techniques	U20PE770EC	Digital Image and Video Processing	U20PE780EC	Network Management
Professional Elective – IV	U20PE790EC	VLSI Physical Design	U20PE711EC	Satellite Communication	U20PE721EC	Biomedical Signal Processing	U20PE731EC	Voice and Data Networks
VIII – Semester								
Professional Elective – V	U20PE810EC	Low Power VLSI Design	U20PE820EC	Global Positioning System	U20PE830EC	Image and Video processing using Machine Learning	U20PE840EC	Optical Networks
Professional Elective – VI	U20PE850EC	Real Time Systems	U20PE860EC	Radar and Navigation Systems	U20PE870EC	Adaptive Signal Processing	U20PE880EC	Software Defined and Cognitive Radio networks