

**VASAVI COLLEGE OF ENGINEERING  
(AUTONOMOUS)**

ACCREDITED BY NAAC WITH 'A++' GRADE

Ibrahimbagh, Hyderabad-31

Approved by A.I.C.T.E., New Delhi and

Affiliated to Osmania University, Hyderabad-07

**Sponsored**

**by**

**VASAVI ACADEMY OF EDUCATION**

**Hyderabad**



**SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR**

**Bachelor of Engineering (ECE)**

**with**

**Honours Program in System on Chip Design**

**With effect from 2023-24**

**(For the batch admitted in 2021-22)**

**(R-21)**



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Phones: +91-40-23146040, 23146041

Fax: +91-40-23146090

## **Institute Vision**

Striving for a symbiosis of technological excellence and human values

## **Institute Mission**

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

## **Department Vision**

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering and fostering ethical values

## **Department Mission**

To inculcate a spirit of scientific temper and analytical thinking and train the students in contemporary technologies in Electronics and Communication Engineering to meet the needs of the industry and society with ethical values

<b>B.E (ECE) Program Educational Objectives (PEO's)</b>	
<b>PEO I</b>	Graduates will be able to identify, analyze and solve engineering problems.
<b>PEO II</b>	Graduates will be able to succeed in their careers, higher education, and research.
<b>PEO III</b>	Graduates will be able to excel individually and in multidisciplinary teams to solve industry and societal problems.
<b>PEO IV</b>	Graduates will be able to exhibit leadership qualities and lifelong learning skills with ethical values.

<b>B.E. (ECE) PROGRAM OUTCOMES (PO's)</b>	
<b>Engineering Graduates will be able to:</b>	
<b>PO1</b>	Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
<b>PO2</b>	Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
<b>PO3</b>	Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal and environmental considerations.
<b>PO4</b>	Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.
<b>PO5</b>	Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
<b>PO6</b>	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
<b>PO7</b>	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
<b>PO8</b>	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
<b>PO9</b>	Individual and team work: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
<b>PO10</b>	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
<b>PO11</b>	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
<b>PO12</b>	Lifelong learning: Recognize the need, and for have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

**B.E (ECE) PROGRAM SPECIFIC OUTCOMES (PSO's)**

<b>PSO I</b>	ECE students will be able to analyze and offer circuit and system level solutions for complex electronics engineering problems, keeping in mind the latest technological trends.
<b>PSO II</b>	ECE students will be able to apply the acquired knowledge and skills in modeling and simulation of communication systems.
<b>PSO III</b>	ECE students will be able to implement signal and image processing techniques for real time applications.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION **(R-21)**

## Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

B.E (ECE) Honours Degree in SoC Design										
S. No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits	Semester
			Hours per Week			Duration in Hrs	Maximum Marks			
			L	T	P		SEE	CIE		
1	U21PC550EC	FPGA Based System Design	3	-	-	3	60	40	3	V
2	U21PC551EC	FPGA Based System Design Lab	-	-	2	3	50	30	1	V
3	U21PC650EC	Advanced System Design	3	-	-	3	60	40	3	VI
4	U21PC651EC	Advanced System Design Lab	-	-	2	3	50	30	1	VI
5	U21PC730EC	Design Verification	3	-	-	3	60	40	3	VII
6	U21PC731EC	Design Verification Lab	-	-	2	3	50	30	1	VII
7	U21PW729EC	Course Project	-	-	6	3	50	50	3	VII
<b>Total</b>			<b>9</b>	<b>-</b>	<b>12</b>		<b>380</b>	<b>260</b>	<b>15</b>	
<b>Grand Total</b>			<b>21</b>				<b>640</b>			
8	NPTEL Courses : SoC related 1 NPTEL course with 12 weeks duration								<b>3</b>	V to VII
<b>Total Credits</b>									<b>18</b>	
<b>Note:</b> Students willing to Opt B.E (ECE) Honours Degree in System on Chip Design shall complete one NPTEL Course Certification (equivalent to 2 Credits weightage) by the end of IV-Semester.										

**NPTEL Courses Recommended by the ECE Department (R-21)**

<b>S.No.</b>	<b>Title</b>	<b>Instructor</b>	<b>Name of the College</b>	<b>Duration</b>
1	Embedded System Design with ARM	Prof. Indranil Sengupta Prof. Kamalika Dutta	IIT Kharagpur	12 weeks
2	Digital VLSI Testing	Prof. Santanu Chattopadhyay	IIT Kharagpur	12 weeks
3	Analog IC Design	Dr. Nagendra Krishnapura	IIT Madras	12 weeks
4	CMOS Analog VLSI Design	Prof. A.N. Chandorkar	IIT Bombay	12 weeks
5	VLSI Physical Design	Prof. Indranil Sengupta	IIT Kharagpur	12 weeks
6	VLSI Design Verification and Test	Dr. Santosh Biswas Prof. Jatindra Kumar Deka	IIT Guwahati	12 weeks
7	C-Based VLSI Design	Prof. Chandan Karfa	IITG	12 Weeks

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## FPGA Based System Design

SYLLABUS FOR B.E. V - SEMESTER

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: <b>U21PC550EC</b>
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The objective of the course is to enable students to apply their knowledge in designing digital systems using integrated circuit cells as building blocks and employing hierarchical design methods with the help of EDA tools. Emphasis is given on digital design using Verilog HDL and FPGA architectures	On completion of the course, students will be able to <ol style="list-style-type: none"> <li>1. Design and model combinational circuits with Verilog HDL at different levels.</li> <li>2. Design and analyse various sequential digital circuits by Verilog HDL.</li> <li>3. Understand the different FSM coding styles and Timing &amp; CDC concepts</li> <li>4. Analyse different types of FPGAs and their modules.</li> <li>5. Understand the Project Design using ZYNQ board.</li> </ol>

### CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3											2		
CO2	2	2	1										2		
CO3	2	2	1		2								2		
CO4	2	2	1		2								2		
CO5	2	2	1		2								2		

### UNIT-I:

Overview of combinational circuits and sequential Circuits, Maximum frequency calculation, set up & Hold time, Clock Skew, Jitter, Propagation Delay, Request load control system

### UNIT-II:

Blocking and nonblocking assignments in Verilog, Verilog Modelling of Combinational Circuits like Adders, Multipliers, Parity Generator Comparators and sequential circuits like Realization of Shift Registers, Realization of a Counter

**UNIT-III:**

FSM coding styles: Binary, one hot encoding, 1 Always block, 2 Always block, 3 Always block and comparisons among them. FSM based Applications. Clock Domain Crossing, Sync and Async FIFO, FIFO depth calculation

**UNIT-IV:**

FPGA general description, Different kinds of FPGA packages, FPGA architecture, Internal hardware modules of FPGA, their meanings and usage, Basic building blocks, Different kinds of I/O modules.

**UNIT-V:**

Zynq Architecture design, Anti fuse, SRAM and EPROM based FPGAs, Project design using Verilog Hardware Description Language (HDL), Verilog Coding and Simulation of Digital Systems. Implementation examples of Logic functions using LUTs and CLBs

**Learning Resources:**

1. Pong P Chu, "FPGA Proto Typing by Verilog Examples" WILEY Publications.
2. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
3. Steve Kilts "Advanced FPGA Design: Architecture, Implementation, and Optimization", WILEY Publications.
4. Verilog HDL: A Guide to Digital Design and Synthesis – by Samir Palnitkar, Prentice Hall PTR Publishers

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests :  Max. Marks for each Internal Test :
2. No. of Assignments :  Max. Marks for each Assignment :

Duration of Internal Test: 90 Minutes



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## FPGA Based System Design Lab

SYLLABUS FOR B.E. V SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: <b>U21PC551EC</b>
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
The objective of the course is to enable students to apply their knowledge for the design of complex high-speed digital circuits and implement them using FPGA.	On completion of the course, students will be able to 1. Learn to write HDL code for simulation and synthesis. 2. Analyse and understand different combinational and Sequential Circuit examples and use the existing examples for new designs. 3. Analyse and Understand the timing and utilization for the implemented designs.

### CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3			2								2		
CO2	2	2			2								2		
CO3	2	2			2								2		

### List of Experiments:

1. FPGA Design flow using Vivado Tools.
2. Design & Implementation of Combinational Circuit
3. Design & Implementation of n-bit Comparator.
4. Test Bench Creation and Simulation of Synchronous circuit
5. Design and Implementation of FSM.
6. Design and Implementation of FIFO
7. Memory Design and Implementation.
8. Mini Project.

**References:** <https://reference.digilentinc.com/reference/programmable-logic/zedboard/reference-manual>

The break-up of CIE:

- |   |   |    |
|---|---|----|
| 1. No. of Internal Test                       | : | 1  |
| 2. Max. Marks for internal tests              | : | 12 |
| 3. Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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## Advanced System Design

SYLLABUS FOR B.E. VI – SEMESTER

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: <b>U21PC650EC</b>
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Justify the philosophy of ARM core as CPU in SoC designs. 2. Demonstrate ARM ISA Assembly usage for data processing. 3. Implement and Debug embedded drivers in C for Cortex M4 MCU.	On completion of the course, students will be able to 1. Summarize ARM based SoC design principles for efficient system design. 2. Describe Cortex M4 Core Architecture and Interrupt processing. 3. Construct programs using ARM ISA Assembly for data processing needs. 4. Design & Validate embedded C drivers for on-chip peripherals of STM32. 5. Realize a complete system using ARM Cortex M4 with different I/Os.

### CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2	2	1	2							1	2	2	1
CO2	2	2	2	1	2							1	2	2	1
CO3	3	2	3	2	3				1			1	2	2	1
CO4	3	2	3	2	3				1	1		1	2	2	1
CO5	1	2	3	1	2				2	1		1	2	2	1

### UNIT-I:

#### Introduction to Advanced System Design (ARM Cortex IP)

The ARM RISC design philosophy, System hardware – AMBA bus, System software; ARM registers bank, status registers; vector table, data flow model. ARM Cortex MCU Echo system

### UNIT-II:

**ARM Instruction Set Architecture (ARM ISA):** ARM Architecture and Assembly Language Programming: The General-purpose Registers in the

ARM, The ARM Memory Map; Load and Store Instructions in ARM; ARM CPSR; ARM Data Format and Directives ARM Addressing Modes

**UNIT-III:**

**SoC Programming (STM32F4):** STM32F4 Microcontroller; Memory mapping of STM32F GPIO Programming and Interfacing; Seven Segment LED Interfacing & Programming; BCD display interfacing

**UNIT-IV:**

**STM ARM Timer Programming:** Introduction to Timers and Counters; System Tick Timer, Timer and delay generation in STM32F4xx

UART: Introduction to serial communication, Programming UART Ports, Usage of Console I/O drivers in C

**UNIT-V:**

**ARM Interfacing with Real World:**

Matrix Keypad; LCD – Design options with 4-bit mode and 8-bit modes; DC Motor & Stepper Motor interfacing designs in Embedded-C. Application development in Embedded C++; debugging methods.

**Learning Resources:**

1. ARM System-on-chip Architecture by Steve Furber, Pearson Education, ISBN978-81-317-0840-8, 2E, 2012.
2. STM32 ARM Programming for Embedded Systems, Muhammad Ali Mazidi, Shujen Chen, Eshragh Ghaemi ISBN: 978-099-792-5944, 2018
3. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®-M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests :  Max. Marks for each Internal Test :
2. No. of Assignments :  Max. Marks for each Assignment :

Duration of Internal Test: 90 Minutes

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## Advanced System Design Lab

SYLLABUS FOR B.E. VI SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: <b>U20PC651EC</b>
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
1. Execute ARM assembly programs for data processing needs. 2. Design electronic systems with Cortex M4 MCUs 3. Design and Realize a System Design using embedded C with ARM Cortex M4 MCU.	On completion of the course, students will be able to 1. Implement ARM assembly data processing instructions for Cortex M4. 2. Construct programs & Validate designs using cross assembler & compiler. 3. Develop embedded C drivers for on-chip peripherals of STM32F411RE. 4. Design system level solutions with off-chip components in Proteus 5. Realize a complete system using ARM Cortex M4 with different I/Os.

### CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	3	2	3				1	1	1	1	3	2	1
CO2	3	2	3	2	3				1	1	1	1	3	2	1
CO3	3	2	3	2	3				1	1	1	1	3	2	1
CO4	3	2	3	2	3				1	1	1	1	3	2	1
CO5	3	2	3	2	3				1	1	1	1	3	2	1

### Module – 1 (ARM Cortex M4 Assembly Language Programming)

1. ARM Data formats and Directives.
2. Addressing Modes.
3. Arithmetic & Logical instructions.
4. Looping and Branching Instructions.
5. Conditional Subroutines.
6. ARM Time Delay and instruction pipeline instructions.
7. ARM Conditional Execution of Assembly.

**Module-2 (STM32F4xxx MCU based SBC)**

1. GPIO Programming.
2. Timer Programming.
3. Interfacing 7-segment display.
4. Full duplex UART Driver design in Embedded C.
5. Interfacing a 4x4 Matrix keyboard for input and 2x16 LCD for output.
6. ADC Driver design for interfacing a Sensor.
7. DAC driver design for generating different signals for control system applications.

The break-up of CIE:

- |   |   |    |
|---|---|----|
| 1. No. of Internal Test                       | : | 1  |
| 2. Max. Marks for internal tests              | : | 12 |
| 3. Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**Design Verification**

**SYLLABUS FOR B.E. VII – SEMESTER**

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: <b>U21PC730EC</b>
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

<b>COURSE OBJECTIVE</b>	<b>COURSE OUTCOMES</b>
1. To provide detailed knowledge in VLSI design process starting from digital design, hardware descriptive languages, synthesis, simulation, verification, FPGA programming & implementation. 2. Will understand the entire logic design process and will be able to take the challenges posed by the chip design industry.	On completion of the course, students will be able to 1. Write Verilog code, and execute sequential circuits on any VLSI design platform. 2. Perform verification and testing. 3. Understand and use the System Verilog design and synthesis features. 4. Apply the System Verilog verification features including Structures and classes. 5. Demonstrate the designs having a set of objective criteria and design constraints.

**CO-PO-PSO Mapping:**

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2	2										2	2	
CO2	1	2	2		2								2	2	
CO3	2	2	2										2	2	
CO4	1	2	2	2									2	2	
CO5	1	2	2	2	2								2	2	

**UNIT-I:**

Blocking and nonblocking assignments in Verilog; Modeling of sequential circuits (Decade Counters, Binary counters, binary sequence detection etc) using Verilog; Writing test benches for these designs; The importance of verification in ASIC design, Functional verification approaches.

**UNIT-II:**

Verification coverage – statement-, block-, branch-, expression-, and FSM-coverage. Verification tools and verification plan; Architecting test benches; Writing basic self-checking test benches; role of tasks and

functions in test benches; automatic tasks and functions; Understanding fork-join execution.

**UNIT-III:**

System Verilog as a Hardware Design & Verification Language (HDVL); SV language elements, data types, enumeration types, arrays and dynamic arrays, queues, strings.

**UNIT-IV:**

Structures and classes, SV operators and expressions; Transaction class, Randomization of stimulus; generator class, driver class, scoreboard class, monitor class, checker class; Basic testbench in System Verilog.

**UNIT-V:**

Threads and interprocess communication, Advanced OOP and test bench guidelines, A complete SV test bench.

**Learning Resources:**

1. Verilog HDL: A Guide to Digital Design and Synthesis – by Samir Palnitkar, Prentice Hall PTR Publishers.
2. System Verilog for Verification – a guide to learning the Testbench language features; 2nd edition or 3rd edition– by Chris Spear; Springer Verlag Publications.
3. A System Verilog Primer – by J Bhaskar; BS Publications, India.
4. Writing Testbenches – Functional verification of HDL models; 2nd edition by Janick Bergeron; Kluwer Academic Publishers

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests :  Max. Marks for each Internal Test :
  2. No. of Assignments :  Max. Marks for each Assignment :
- Duration of Internal Test: 90 Minutes

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**Design Verification Lab**

SYLLABUS FOR B.E. VII SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: <b>U21PC731EC</b>
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
To perform design and verification of different applications of sequential circuits.	On completion of the course, students will be able to 1. Design various sequential circuits using HDL. 2. Write test benches for the simulation of sequential circuits. 3. Verification of design using system Verilog.

**CO-PO-PSO Mapping:**

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2	2		3								2	2	
CO2	2	2			3								2	2	
CO3	2	2	2		3								2	2	

**Laboratory Experiments:**

1. Writing Verilog code for sequence detector FSM and running simulation.
2. Verilog coding of the sequence detector using Shift register.
3. Verilog based Design of a decade counter and other special counters.
4. Writing test bench and verifying the working of a Decade Counter.
5. Writing design code in Verilog for a "Candy Vending Machine" problem.
6. Writing test bench using Tasks, and verify the working of the candy vending machine.
7. Measuring the verification coverage of the test bench for Candy Vending Machine.
8. Writing design code for the Washing Machine Controller problem.
9. Writing directed tests in the test bench for Washing Machine Controller and measuring the coverage.



10. Porting the test bench of Candy Vending Machine to System-Verilog (SV) - phase-1.
11. Porting the test bench of Candy Vending Machine to System-Verilog (SV) - phase-2.
12. Measuring verification coverage of the Candy Vending machine Test bench.
13. Porting the test bench of Washing Machine Controller to SV - phase-1
14. Porting the test bench of Washing Machine Controller to SV - phase-2.

The break-up of CIE:

- |   |   |    |
|---|---|----|
| 1. No. of Internal Test                       | : | 1  |
| 2. Max. Marks for internal tests              | : | 12 |
| 3. Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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**Course Project**

**SYLLABUS FOR B.E. VII SEMESTER**

L:T:P (Hrs./week) : 0:0:6	SEE Marks : 50	Course Code: <b>U21PW729EC</b>
Credits : 3	CIE Marks : 50	Duration of SEE : 3 Hours

<b>COURSE OBJECTIVES</b>	<b>COURSE OUTCOMES</b>
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design.	On completion of the course, students will be able to <ol style="list-style-type: none"> <li>1. To select the complex engineering problems beneficial to the industry &amp; society and develop solutions with appropriate considerations.</li> <li>2. To apply modern tools and analyze the results to provide valid conclusions.</li> <li>3. To communicate effectively the solutions with report and presentation following ethics.</li> <li>4. To work in teams and adapt for the advanced technological changes</li> <li>5. To apply management principles to complete the project economically</li> </ol>

**CO-PO/PSO Mapping**

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3	3			2	2								
CO2				3	3										
CO3								3		3					
CO4									3			3			
CO5											3				

**Note:** CO1 & CO2 must be mapped with one of the relevant PSOs based on the domain of the project with 3  
CO4 can be mapped to appropriate PSO with level 2

Oral presentation is an important aspect of engineering education. The objective of the course project is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design.

Project topics may be chosen by the student with advice and approval from the faculty members. Students are to be assessed and evaluated as per the following criteria.

- Selection of topic & Literature survey
- Solution & Clarity in Implementation
- Modern tool usage in Implementation
- Results and Analysis
- Team Work, Report writing & Presentation with ethics
- Project Management

**Each student is required to:**

1. Submit a one-page synopsis in the beginning of project work for display on the notice board.
2. Give a 20 minutes presentation through LCD power point presentation followed by a 10 minutes discussion.
3. Submit a report on the project work with list of references and slides used.

Project reviews are to be scheduled from the 3<sup>rd</sup> week of the semester to the last week of the semester and any change in schedule should be discouraged.

- Batch size shall be 2 to 3 students.
- Allocation and finalization of the projects by department.
- Two reviews – One during 5<sup>th</sup> week and another during 10<sup>th</sup> week and final evaluation shall be conducted during 15<sup>th</sup> to 16<sup>th</sup> week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.