Scheme of Instruction & Scheme of Examination

(Subjected to the approval of Osmania University, Hyderabad)

Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

Applicable for the students to be admitted in A.Y. 2020-21 (R-20)

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) HYDERABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

SCHEME OF INSTRUCTION AND EXAMINATION (R-20)

(Subjected to the approval of Osmania University, Hyderabad)

Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

B.E (ECE) Honor's Degree in SoC Design											
S. No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination				Credits	Semester
			Hours per Week			Duration in Hrs	Maximum Marks				
			L	T	P		SEE	CIE			
THEORY cum PRACTICALS											
1.	U20PC550EC	Advanced Computer System Design : Theory cum Lab	2	-	2	3	60	40		3	V
2.	U20PC650EC	Field Programmable Gate Array (FPGA) Based System Design : Theory cum Lab	2	-	2	3	60	40		3	VI
3.	U20PC730EC	System on Chip Design and Verification: Theory cum Lab	2	-	2	3	60	40		3	VII
4.	U20PW729EC	Minor Project	-	-	6	3	60	40		3	VII
		TOTAL	**6**	**-**	**12**	**-**	**240**	**160**		**12**	
		GRAND TOTAL	**18**				**400**				
5.	MOOCs Courses (SoC related) : 8 or 12 weeks durations									6	V to VII
									Total Credits	**18**	