Presentation

on

Course Structure, Scheme of Instruction & Scheme of Examination

Bachelor of Engineering (ECE)
with Honours Degree in System on Chip Design

Applicable for the students to be admitted in A.Y. 2020-21 (R-20)

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

(ACCREDITED BY NAAC WITH 'A++' GRADE)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) :: (ACCREDITED BY NAAC WITH 'A++' GRADE)

SCHEME OF INSTRUCTION AND EXAMINATION (R-20)

Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

B.E (ECE) Honours Degree in SoC Design										
S. No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits	Semester
			Hours per Week			Duration in Hrs	Maximum Marks			
			L	T	P		SEE	CIE		
1.	U20PC550EC	Advanced System Design	2	-	-	3	60	40	2	V
2.	U20PC551EC	Advanced System Design Lab	-	-	2	3	50	30	1	V
3.	U20PC650EC	Field Programmable Gate Array (FPGA) Based System Design	2	-	-	3	60	40	2	VI
4.	U20PC651EC	Field Programmable Gate Array (FPGA) Based System Design Lab	-	-	2	3	50	30	1	VI
5.	U20PC730EC	Design Verification	2	-	-	3	60	40	2	VII
6.	U20PC731EC	Design Verification Lab	-	-	2	3	50	30	1	VII
7.	U20PW729EC	Course Project	-	-	6	3	60	40	3	VII
		TOTAL	**6**	**-**	**12**	**-**	**390**	**250**	**12**	
		GRAND TOTAL	**18**				**640**			
8.	NPTEL Courses : SoC related 2 NPTEL courses with 12 weeks duration								6	V to VII
								Total Credits	**18**	

Note: Students willing to Opt B.E (ECE) Honours Degree in System on Chip Design shall complete one NPTEL Course Certification (equivalent to 2 Credits weightage) by the end of IV-Semester.