

VLSI DESIGN LAB MINI PROJECT

4 BIT ARRAY MULTIPLICATION

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AIM: To Design and verify 4 bit array multiplication.

APPARATUS: Cadence Virtuoso, ADE

MOTIVATION TO DO PROJECT:

The motivation behind implementing a 4-bit array multiplier in VLSI (Very Large Scale Integration) can be driven by several factors and considerations:

Low Power Consumption: Array multipliers are known for their low power consumption compared to other multiplier architectures. This is crucial in modern VLSI design where power efficiency is a critical concern.

Area Efficiency: Array multipliers have a regular structure, making them area-efficient. This is beneficial in VLSI design where the efficient use of silicon real estate is essential to reduce manufacturing costs and increase the number of components on a chip.

Parallelism: Array multipliers inherently provide parallelism by breaking down the multiplication process into smaller, independent tasks. This can result in faster multiplication operations, a significant advantage in applications where speed is crucial.

Scalability: The 4-bit size is chosen for simplicity, but the array multiplier can be easily scaled to handle larger bit sizes. This scalability is advantageous when designing components for various applications that may require different word lengths.

Educational Purposes: Implementing a 4-bit array multiplier is often used in educational settings to teach VLSI design principles, digital logic, and arithmetic operations. It provides hands-on experience in designing and understanding basic building blocks of digital systems.

Compatibility: In certain applications, especially those involving legacy systems or specific communication protocols, a 4-bit multiplier may be sufficient. Implementing a 4-bit array multiplier ensures compatibility with such systems.

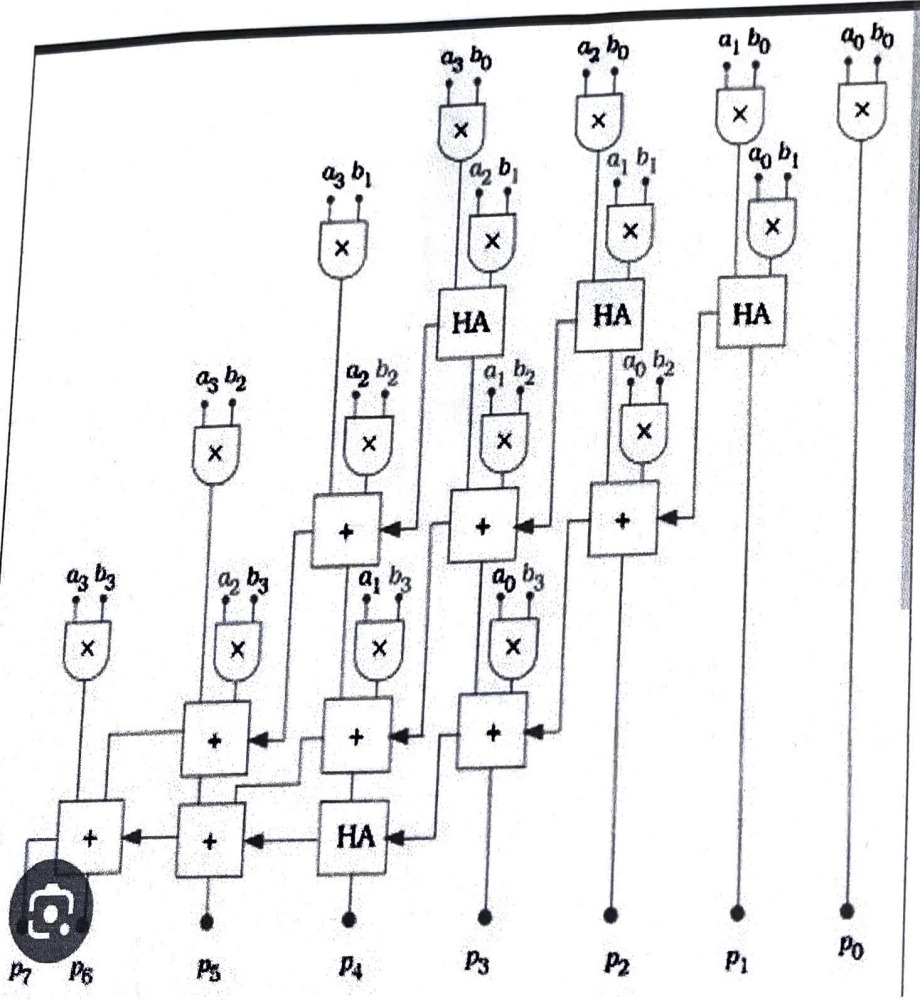
Customization: Designing a 4-bit array multiplier allows for customization based

on specific application requirements. Different multiplication algorithms or optimizations can be explored and implemented to meet the unique needs of a particular system.

Research and Development: Researchers may choose to work on 4-bit array multipliers as part of a broader study in the field of digital design, VLSI architecture, or optimization algorithms. It can serve as a foundational component for more advanced research.

Ultimately, the motivation for implementing a 4-bit array multiplier in VLSI lies in achieving a balance between power efficiency, area utilization, and performance based on the specific requirements of the target application or educational context.

BLOCK DIAGRAM



WORKING :

An array multiplier is a digital circuit used in Very Large Scale Integration (VLSI) design for multiplying two binary numbers. It utilizes an array of binary adders and partial product generators to perform the multiplication operation efficiently. The array multiplier architecture is commonly used for parallel multiplication to improve speed and throughput.

Here's a basic overview of how an array multiplier works:

1. partial product Generation
2. Partial product Addition
3. Binary Addition
4. Final Sum

EXAMPLE:

$$\begin{array}{r} 1010 \\ X\ 1011 \\ \hline 1010 \\ 1010X \\ 0000XX \\ 1010XXX \\ \hline 1101110 \end{array}$$

SCHEMATIC DIAGRAM:

