DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Vasavi College of Engineering (A), Hyderabad 500031

SCHEME OF INSTRUCTION AND EXAMINATION FOR
M.E. (ECE) – ES&VLSID
With effect from Academic year 2016-17

Sl. No.	Category	Subject code	Subject Title	Scheme of Instruction			Scheme of Examination			Total	Credits
				L	T	P	Duration in Hrs	CIE	Sem end Exam		
I – SEMESTER											
Theory											
1.	PC		Professional Core	3	0	0	3	30	70	100	3
2.	PC		Professional Core	3	0	0	3	30	70	100	3
3.	PC		Professional Core	3	0	0	3	30	70	100	3
4.	PE		Professional Core / Elective	3	0	0	3	30	70	100	3
5.	PE		Professional Elective	3	0	0	3	30	70	100	3
6.	PE		Professional Elective	3	0	0	3	30	70	100	3
7.	EEC		Finishing School - I: Soft Skills	2	0	0	2	15	35	50	1
Laboratory											
8.	PC		Design and Simulation Laboratory-I	0	0	3	3	25	0	25	2
9.	PC		Embedded Systems Laboratory	0	0	3	3	25	0	25	2
10.	EEC		Seminar - I	0	0	2	0	25	0	25	1
				20	0	8	-	270	455	725	**24**
II – SEMESTER											
Theory											
1.	PC		Professional Core	3	0	0	3	30	70	100	3
2.	PC		Professional Core	3	0	0	3	30	70	100	3
3.	PC		Professional Core / Elective	3	0	0	3	30	70	100	3
4.	PE		Professional Elective	3	0	0	3	30	70	100	3
5.	PE		Professional Elective	3	0	0	3	30	70	100	3
6.	PE		Professional Elective	3	0	0	3	30	70	100	3
7.	EEC		Finishing School – II: Soft Skills	2	0	0	2	15	35	50	1
Laboratory											
8.	PC		Design and Simulation Laboratory-II	0	0	3	3	25	0	75	2
9.	PC		Embedded Systems Applications Laboratory	0	0	3	3	25	0	75	2
10.	EEC		Seminar -II	0	0	2	0	25	0	25	1
				20	0	8	-	270	455	725	**24**
III – SEMESTER											
1.	PC		Dissertation seminar	0	0	4	0	50	0	50	2
2.	PC		Dissertation – Phase I	0	0	16	0	100	0	100	8
				0	0	20	-	150	0	150	**10**
IV - SEMESTER											
1.	PC		Dissertation – Phase II	0	0	30	-	Viva-voce (Grade)			15
				0	0	30	-	--			**15**

S.No	Syllabus Ref. No	Subject	Periods per week
Professional Core Subjects			
1	EC 5000	Embedded Systems Design	3
2	EC 5001	Digital IC Design	3
3	EC 5002	Analog IC Design	3
4	EC 5003	Mixed Signal IC Design	3
5	EC 5004	Embedded Real Time Operating Systems	3
6	EC 5005	Physics of Semiconductor Devices	3
7	EC 5007	Design and Simulation Laboratory-I	3
8	EC 5017	Embedded Systems Laboratory	3
9	EC 5027	Design and Simulation Laboratory-II	3
10	EC 5037	Embedded Systems Applications Laboratory	3
11	EC 5018	Seminar – I	3
12	EC 5028	Seminar – II	3
13	EC 5038	Dissertation seminar	4
14	EC 5019	Dissertation – Phase I	16
15	EC 5029	Dissertation – Phase II	30
Professional Electives : VLSI Design			
16	EC 5100	Low Power VLSI Design	3
17	EC 5101	Design For Testability	3
18	EC 5102	VLSI Physical Design	3
19	EC 5103	Principles of VLSI System Design	3
20	EC 5104	Advanced Computer Organization	3
21	EC 5105	CPLD & FPGA Architectures and Applications	3
22	EC 5106	VLSI Technology	3
23	EC 5110	MEMS	3
24	EC 5111	Integrated Optics & Photonic Systems	3
25	EC 5112	RFIC Design	3
26	EC 5113	High Level Synthesis	3
Professional Electives : Embedded Systems			
27	EC 5200	System on Chip Architecture	3
28	EC 5201	Scripting Languages for Embedded Systems	3
29	EC 5202	Internet of Things	3
30	EC 5203	Graph Theory and Its Applications to VLSI	3
31	EC 5204	System Design and Reliability	3
32	EC 5205	Hardware-Software Co-design	3
33	EC 5206	Electromagnetic Interference & Compatibility	3
34	EC 5210	Design of Fault Tolerant Systems	3
35	EC 5211	Reconfigurable System Design	3
36	EC 5212	Soft Computing Techniques	3
37	EC 5213	Low Power Embedded Systems Design	3

EC 5000

EMBEDDED SYSTEMS DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Embedded Systems Overview: Definition of Embedded System; Examples; Design Challenges– Optimizing Design Metrics; Selection of processor or controller & memories; Processor Technology; RISC Vs CISC

UNIT – II

Real World Interfacing using Embedded C with AT89S52 (8051 Microcontroller): ADC0808, LED, Seven Segment Displays, DAC, LCD, Keypad, RTC, DC Motor, Stepper
Motor driving actuators using PWM.

UNIT – III

ARM Core Architecture: Introduction to RISC concepts with ARM as CPU, ARM engine Architecture, AMBA Bus, Core Registers, Programming Modes, Importance of Thumb Mode, CPSR, SPSR, Pipeline, Exceptions, Interrupts and vector table; ARM Programming Model; Core Extensions, ARM Revisions, ARM processor families and comparisons.

UNIT – IV

Embedded Networking: Serial protocols topology & working principles and frame formats – I^2C; SPI; USB; CAN; Ethernet; Parallel Protocols – PCI; PCIx; AMBA bus

UNIT – V

Embedded Debugging Techniques: Debugging Methods using Software and Hardware; usage of JTAG adaptor for ARM and Embedded ICE Embedded Software Architectures Introduction: Round-Robin; RR with Interrupt; Functional Queue Scheduling & need of RTOS

Suggested Reading:

1. Frank Vahid, Tony Givargis “Embedded System Design – A Unified Hardware/Software Introduction” John Wiley & Sons, Inc. 2002.
2. Andrew N Sloss, Dominic Symes & Chris Wright, “ARM System Developer's Guide: Designing and Optimizing System Software”, The Morgan Kaufmann Series 2004.
3. Mazidi M.A and Mazidi J.G, “The 8051 Microcontroller and Embedded Systems”, Pearson 2007.
4. David E Simon, “An Embedded Software Primer”, Pearson Education, 2005

EC 5001

DIGITAL IC DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT- I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, MOSFET secondary effects, Simple Interconnect Wire models, Design rules, Sub-threshold Conduction. CMOS Inverter – Static and Dynamic Behaviour, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis, Detailed Load Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

UNIT - II

Designing Combinational Logic in CMOS: Static CMOS design: Complimentary CMOS, Ratioed Logic, Pass Transistor Logic, Transmission Gate Logic, Optimizing Paths with Logical effort.
Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic, Signal Integrity Issues, Cascading Dynamic Gates

UNIT - III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles, Pipelining to optimize Sequential Circuits, Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic, Advanced Interconnect Techniques, Power Grid and Clock design: Power Distribution Design, Clocking and Timing Issues, Phase-Locked Loops / Delay Locked Loops.

UNIT - IV

Designing Arithmetic Building Blocks: Datapaths in Digital Processor Architectures,: The Adder, The Multiplier, The Shifter and The Comparator. Power and Speed Trade offs in Datapath Operators: Design-Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues

UNIT - V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, SRAM Cell Layout,

Topics beyond syllabus

*Advanced Topics in Memory Design: Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies, PLLS and DLLs

Suggested Reading:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, “Digital Integrated Circuits – A Design Perspective””, Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, “Analysis and Design of Digital Integrated Circuits in DSM Technology”, 3rd Edition, Tata McGraw Hill, 2008.

EC 5002

ANALOG IC DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – 1

Introduction: What are electronic devices and circuits - Types of electrical signals - Characteristics of analog signals - Analog functions - Devices characteristics needed to perform these functions. Discrete component approach to analog circuit - Integrated circuit approach, silicon as base material. Integrated circuit – Components for ICs - Resistors, Capacitors, inductors diodes, BJTS, MOSFETS - Their IC architectures, limitations, circuits design philosophies - Different families of circuits device models. Basic analog circuits - Amplifiers - Different type of loads - Biasing techniques - current mirrors - Coupling techniques between stages.

UNIT – II

Biasing techniques: Basic current mirror architecture - Specifications of current mirrors - Cascode current mirrors - Wide swing current mirrors Wilson current mirror - Degenerate current sources - peaking current sources for very low current biasing - enhanced output impedance current mirrors, Sensitivity analysis of current. Mirrors: Voltage references - VBE, VT and Zenner diode based references, Band gap reference

UNIT – III

Single stage amplifiers CS, CG, CD amplifiers with resistive, diode, current source, and current mirror loads – performance analysis of these circuits – input, output, current and voltage gains at low frequencies swing, frequency response and phase response of these amplifiers, Multistage amplifiers and biasing and swing problems. Cascode amplifiers - Folded cascade amplifiers - Swing analysis. Differential amplifiers, biasing and analysis of performance, Specifications - common and differential mode gain - common mode rejection ratio power rejection ratio, swing differential input differential output amplifier, differential input single ended output amplifier variable gain amplifiers Noise in amplifiers.

UNIT – IV

Operational amplifiers - characteristics and specifications - Two and three stage Op-Amps - analysis of gain, frequency and phase response - Coupling problems, fully differential amplifiers - Cacodes, folded cascodes - common mode feedback, and circuits, active cascade Op-Amp - current differential amplifiers – current feedback Op-Amps, - Gilbert Cells. OTAS.

UNIT – V

Oscillators and mixers: Basics of oscillators - Feedback oscillators, negative resistance oscillators, (two port oscillators), ring oscillators - Differential ring oscillators, LC oscillators, relaxation oscillators, voltage controlled oscillators, Tuning delay and frequency.

Suggested reading:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

EC 5003

MIXED SIGNAL IC DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction: concepts involved in mixed signal circuits - Analog & digital operations by the same circuit - Digital and analog circuits on the same substrate - Problems of covering both the types of circuits on the same substrate processes involved in a circuit which has analog / digital signals at the input and digital / analog of the output – mimicking analog components by digital operations (switched capacitor circuits).

Mixed signal functions - comparators sampling and sample and hold operations - Analog to Digital conversion and Digital / Analog conversion – phase and delay locked loops.

UNIT – II

Switched Capacitor Circuits (SCR) - switched capacitor resistor analysis of current and voltage waveforms - S.C.RS in series and parallel - Power dissipation in SCRFET switches charge in injection and clock feed though effects - limitations o f SCRs. Applications of SCR for (i) filters (ii) amplifiers / buffers, Integrators, Voltage multipliers, peak detectors, modulators etc.

Comparators: Basic architecture of a comparator specifications of a comparator op amp based comparator - limitations - modified comparators for improving performance Latched comparators for high speed applications Bi-polar comparators - BiCMOS comparators.

UNIT – III

Sample and hold circuits **-** specifications MOS sample and hold circuits - clock feed through and charge injection problems **-** S/H circuits with transmission gates - high input impedance S/H circuit - S/H circuits with improved slewing - Diode bridge based S/H circuits advantages and disadvantages of bridge based S/H circuits.

Data converters: Data converter fundamentals performance characteristics - Quantization noise.

UNIT – IV

Data converters, architecture: ideal A/D and D/A converters - Nyquist rate and over sampled D/A converters, philosophy and architectures of Nyquist rate D/A and A/D converters - philosophy and architectures of over sampled converters

Nyquist rate D/A converters: Decoder based converters, binary scaled converters, thermometric code converters, hybrid converters. Nyquist rate A/D converter: Integrating converters, successive approximation converters, Flash or parallel converters two step A/D converter, Cyclic A/D converter, pipe lined A/D converter - VCO based A/D converter.

UNIT – V

Architectures of over sampled A/D converter - 1 bit A/D and D/A converters Σ - Δ modulator, noise shaping and noise shaped A/D converter idle tones and dithering - system level description of over sampled A/D and D/A converters

Phase locked loop: What is phase locked loop and its importance in communication and instrumentation electronics - Basic architecture of a PLL - Analog PLL - Digital PLL - Locking limitations - Dynamics of PLL - lock range - Capture range - phase - frequency locked loop-charge pump based PLL - components of PLLs, frequency locked loop - Delay locked loop - applications of PLLs.

Suggested reading:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

EC 5004

EMBEDDED REAL TIME OPERATING SYSTEMS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS; Architecture of RTOS , Kernels – classifications, importance of scheduler in OS: objectives and functions; Hard versus Soft Real-time systems – examples, Jobs & Processes, timing constraints. Preemptive Vs Non preemptive kernels

UNIT – II

Task Priorities, Scheduling, Inter task Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section – Reentrant Functions, Inter Process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

Scheduling Algorithms – RMS, Preemptive EDF scheduling – principle, comparisons.

UNIT – III

Linux Kernel 2.x architecture – File system, Concepts of Process – creation, Process Control Block (PCB); process Vs thread; Concurrent Execution. Process Management in Linux – forks Vs Vfork; process state transitions, zombie state, Memory Management Algorithms.

UNIT – IV

Device Drivers – Definition; advantages of Modules; kernel space Vs user space; Concurrency and Race Conditions; classification of device drivers - character drivers, block drivers and net drivers; shell commands for drivers; IOCTLS and Tasklets

UNIT – V

Communicating with Hardware; Interrupt Handling. Debugging Techniques. Comparison of Linux 2.4 Vs 2.6 & 3.x with RT Linux concepts and porting on hardware. Case study of RTOS-RT Linux porting on LPC2148.

Suggested Reading:

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-to-Use Modules in C”, CMP Publishers Jan 1999.
2. Robert Love, “Linux Kernel Development” (3rd Edition), Novell Press 2010.
3. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
4. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, "Linux Device Drivers", 3rd Edition,O'Reilly Media Publishers
5. Real Time Systems, C.M.Krishna and G.Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

EC 5005

PHYSICS OF SEMICONDUCTOR DEVICES

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Properties of Semiconductors: Crystal Structure Energy Bands, Carrier Transport Phenomena. (Mobility of Carriers, Resistivity and Hall Effect, Generation – Recombination Processes). High Field Phenomena. Gunn Effect and Negative Resistance Characteristics. Equation for Current Flow.

UNIT – II

Bipolar Devices: Ideal P-N Junctions, V-I Characteristics, Effect of Generation – Recombination Processes. Effect of High Injection. Junction Breakdown, Depletion and Diffusion Capacitance. Hetero Junctions. Bipolar Transistor – Characteristics – Equivalent Circuit - Ebers - Moll Model – Gummel Poon Model, Microwave and High Frequency Transistor Structures – Breakdown of Transistors including Secondary Breakdown.

UNIT – III

Field Effect Transistors – JFET, MESFET – Characteristics.

MOSFET and MISFET: MOS Diode – Capacitance Vs Voltage Curves. Interface Trapped Charges – oxide Charge. V-I Characteristics of MIS Diodes with Thin Insulating Films. MOS/MISFET – Different Types – Basic device Characteristics – Sub-threshold Region Characteristics – Buried Channel Devices.

UNIT – IV

Short Channel Effects – On sub-threshold Current, On Threshold Voltage – On the Structures – Shallow Junctions – Breakdown Voltage – Band Gap Engineering – Thin Film Transistor – Silicon On Insulator (SOI) Devices.

UNIT – V

Floating Gate Devices for Non-volatile Memories. MIOS Devices – Gallium Arsenide Devices – Gunn Devices (or Transferred Electron Devices TEDS) – Functional Devices for Microwave Oscillators. LEDS and Laser Diodes.

Suggested Reading:

1. S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, 1981.
2. Dewitt G. ONG., Modern MOS Technology: Processes, Devices and Design,Mc. Graw Hill Book Company. 1984.
3. CHEN , VLSI Hand book, CRC Press, IEEE Press, 2000.

EC 5007

DESIGN AND SIMULATION LABORATORY-I

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Design and simulation of combinational circuits

(ii) Design and simulation of sequential circuits

(iii) Design and simulation of mixed signal circuits

(iv) Microcontroller programming

a. Toggling the LEDs,

b. serial data transmission,

c. LCD and Key pad interface

EC 5017

EMBEDDED SYSTEMS LABORATORY

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

List of Experiments using Embedded C/Embedded C++:

1. To toggle LEDs connected to GPIOs of AT89S52 with some intentional Delay.
2. To design & implement 4x3 matrix Keypad Device Driver for ASCII mapping.
3. To design & implement 2x16 LCD Device Driver for displaying below text:

   Line-1: "**Welcome@ESD Lab!**"

   Line-2:"**Enter to Proceed**"
4. To Configure Timer0 and Timer1 for intended delay without interrupts.
5. To design & demonstrate the UART drivers for data transmission and data reception at 9600bps full duplex baud.
6. To design & implement the concept of writing Interrupt Service Routine (ISR) for external interrupt INT0, INT1.
7. To design & implement the concept of mixing of external ISRs with Internal ISRs and understanding the ISR handling process.
8. To design & implement LED Seven Segment driver with adjustable delay.
9. To design & implement User Centric template Menu designs in Embedded C
10. To design & implement User Centric template Menu designs in Embedded C++.

Suggested tools for use:

1. Hardware Target CPU – AT89S52
2. Embedded Software Development – Keil µVision4 IDE
3. Embedded Debugger – Keil µVision4 Debugger
4. Hardware Simulator – Proteus

Note: The experiments will be decided and modified if necessary and conducted by the lecturer concerned.

EC 5027

DESIGN AND SIMULATION LABORATORY-II

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Synthesis of combinational circuits (4 to 6 MSI digital blocks).

(ii) Synthesis of sequential circuits (4 to 6 MSI digital blocks).

(iii) Schematic simulation, layout, DRC, LVS, parasitic extraction for cells (inverter, NAND gate, NOR gates).

(iv) Programming using real time operating systems

a. Multi tasking using round robin scheduling
b. IPC using message queues
c. IPC using semaphore
d. IPC using mail box

EC 5037

EMBEDDED SYSTEMS APPLICATIONS LABORATORY

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

List of Experiments in RTOS using Embedded – C/C++:

Part – A
Real World Interfacing

1. embOS Real Time Task Creation Demonstration of Multi taksing.
2. Cooperative Scheduling Algorithm (Or) Round Robin Archiecture in RTOS.
3. Preemptive Scheduling Algorithm in embOS.
4. Resource Semaphore (Binary Semaphore) Demonstration.
5. Couting Semaphore IPC among the embOS tasks.
6. Message Queues & Mailboxes in embOS tasks.

Part – B
Mini Project

7. Mini project with the actual realization in the hardware powered with any standard MCUs available and prototying the application hardware.

(Or)

8. Study and implementation of embOS RTOS among the hardware peripharals available and prototyping a hard real time system design with emPower target.

Suggested tools for use :

1. Hardware Target CPU – Cortex M4F powered Segger Board
2. Embedded Software Development – Embedded Studio v 3.12a
3. Embedded Debugger – Cortex M4F ARM J Link
4. Hardware platform – Segger emPower board
5. RTOS – embOS

Note: The experiments may be decided and modified based on additional hardware and/or software tools availability from time-to-time.

EC 5018

SEMINAR - I

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Communication Engineering and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

EC 5028

SEMINAR - II

Instruction	3 Periods per week	External Examination - Duration	-
Sessionals	50 Marks	External Examination - Marks	-
Credits	02		

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Communication Engineering and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

EC 5038

DISSERTATION SEMINAR

Instruction	6 Periods per week	External Examination - Duration	-
Sessionals	100 Marks	External Examination - Marks	-
Credits	06		

The main objective of the Project Seminar is to prepare the students for the dissertation to be executed in 4th semester. Solving a real life problem should be focus of Post Graduate dissertation. Faculty members should prepare the project briefs (giving scope and reference) at the beginning of the 3rd semester, which should be made available to the students at the departmental library. The project may be classified as hardware / software / modeling / simulation. It may comprise any elements such as analysis, synthesis and design.

The department will appoint a project coordinator who will coordinate the following:

- Allotment of projects and project guides.
- Conduct project - seminars.

Each student must be directed to decide on the following aspects

- Title of the dissertation work.
- Organization.
- Internal / External guide.
- Collection of literature related to the dissertation work.

Each student must present a seminar based on the above aspects as per the following guidelines:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through OHP, PC followed by a 10 minutes discussion.
3. Submit a report on the seminar presented giving the list of references.

Project Seminars are to be scheduled from the 3rd week to the last week of the semester.
The internal marks will be awarded based on preparation, presentation and participation.

EC 5019

DISSERTATION – PHASE I

Instruction	--	External Examination - Duration	--
Sessionals	--	External Examination - Marks	Grade+
Credits	10		

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent /Very Good / Good/Satisfactory / Unsatisfactory

EC 5029

DISSERTATION – PHASE II

Instruction	--	External Examination - Duration	--
Sessionals	--	External Examination - Marks	Grade+
Credits	10		

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent /Very Good / Good/Satisfactory / Unsatisfactory

EC 5100

LOW POWER VLSI DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction to Low Power design: Why worry about power – at global and SOC levels, Emerging zero-power applications (WSN), 20 nm scenario, Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels)

Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design – Standby leakage control using transistor stacks, Multiple V_{TH} and dynamic V_{TH} techniques, Supply voltage scaling technique (Ref-1)

UNIT – II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories (Ref-2)

UNIT – III

Power Optimization Techniques – II: Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues (Ref-2)

Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power (Ref-3)

UNIT IV

Low Voltage Low Power Static Random Access memories:

Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, Loadless CMOS 4T SRAM cell, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction (Ref-1)

UNIT V

Large LP VLSI System design and Applications:

Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, Varying the clock speed, varying the V_{DD} of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

Contents beyond Syllabus:

Low Power Design for safety Critical applications: safe operation constraints vs low-power techniques, Unsuitable low power design techniques for safety critical applications, Low-power and safe-operating circuits. (4 hours)

Suggested Reading:

1. Kiat-Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata McGrawhill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, " Low-Power CMOS VLSI Circuit Design" , Wiley Pub., 2000 (Unit III)
4. Dimitrios Soudris, Christian Piguet and Coastas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002 (Topics beyond Syllabus)
5. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010 (for seminars and assignments)

EC 5101

DESIGN FOR TESTABILITY

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction to Test and Design for Testability (DFT) Fundamentals.

Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT – II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT – III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT – IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Suggested Reading:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch., Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

EC 5102

VLSI PHYSICAL DESIGN

Instruction	4 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Scope of physical design – Components of VLSI – Various layers of VLSI – Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

UNIT – II

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Mask overlays for different structures. Parasitics – latch up and its prevention. Device matching and common centroid techniques for analog circuits

UNIT – III

Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT – IV

Cell concepts – cell based layout design – Wein-berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnect delay modeling, floor planning, routing and clock distribution.

UNIT – V

CAD Tools: Layout editors, Design rule checkers, circuit extractors – Hierarchical circuit extractors – Automatic layout tools, silicon compilers, modeling and extraction of circuit parameters from physical layout.

Suggested Reading:

1. Preas, M. Lorenzatti, “Physical Design and Automation of VLSI Systems”, The Benjamin-Cummins Publishers, 1998.
2. M. Shoji, “CMOS Digital Circuit Technology”, Prentice Hall, 1987.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
4. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
5. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.

EC 5103

PRINCIPLES OF VLSI SYSTEM DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction to VLSI System design hierarchical design – design abstraction – different levels of abstraction and domains. Computer aided design VLSI design flow– technology implications and economics, issues connected with technology defect densities yield and die size, components of chips cost.

UNIT – II

Static and dynamic CMOS circuits, circuit characterizations and performance estimation: Resistance, Capacitance and Inductance – delay estimations power dissipation static and dynamic, design margining – reliability issues.

UNIT – III

CMOS design methods: Structured design strategies – Hierarchy, regularity modularity, chip design options: Programmable logic, logic structures: gate arrays, sea – of gate and gate array and standard cell based designs- standard cell libraries including I/O and ESD protection structures, design re- use and full custom mask design.

UNIT – IV

CMOs sub system design: Adders and Subtractors fast adders like carry by pass carry select and carry look ahead adders Multipliers, array and fast multipliers – Parity Generators - Zero-One Detectors – Binary Counters – Multiplexers – shifters – memory elements

UNIT – V

CMOs System case study: Core of RISC Micro Controller ALU address architectures, Instruction sets pipelining major blocks of the processor and 6 Bit Flash A/D Converter – high speed comparators and thermometer code converter.

Suggested Reading:

1. Weste Kamran Eshraghian, Principles of CMOS VLSI design – a Systems Perspective by NEILHE, Pearson Education Series, Asia, 2002.
2. Wolf, Modern VLSI Design, Pearson Education Series, 2002.
3. Jean M. Rabey, " Digital Integrated Circuits", Prentice Hall India, 2003

EC 5104

ADVANCED COMPUTER ORGANIZATION

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Review of Computer Arithmetic: Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating Point Arithmetic.

Processor Design Techniques: Instruction Pipelining, Super Scalar techniques, Linear pipeline processors, Super scalar and super pipeline design, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

UNIT – II

Control Unit Design: Basic Concepts: Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Micro program sequencer, Case studies based on both the approaches.

UNIT – III

Memory Organization: Internal memory, computer memory system overview, the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT – IV

I-O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Bus Arbitration; Synchronous bus and asynchronous bus, Interface circuits, Parallel port, Serial port, standard I/O interfaces, IO Processor, PCI bus, SCSI bus, USB bus protocols.

UNIT – V

Parallel Computer Systems: Instruction Level Parallelism (ILP) – Concept and Challenges, Dynamic Scheduling, Limitations on ILP, Thread Level Parallelism, Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors, SIMD computers and Super computers.

Suggested Reading:

1. William Stallings, Computer Organization and Architecture designing for Performance, 7th edition, PHI, 2007.
2. Carl Hamacher, Vranesic, Zaky, Computer Organization, 5th edition, MGH.
3. Hayes John P; Computer Architecture and organization; 3rd Edition, MGH, 1998.
4. John L. Hennessy and David A. Patterson, Computer Architecture – A quantitative Approach, 3rd Edition, Elsevier, 2005.
5. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

EC 5105

CPLD & FPGA ARCHITECTURES AND APPLICATIONS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT – II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT – III

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT – IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT – V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps.
Verification: introduction, logic simulation, design validation, timing verification.
Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Suggested Reading:

1. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Pearson Education 2009.
2. S. Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S. Brown, R. Francis, J. Rose, Z.Vransic, Field Programmable Gate array, Kluwer Publn, 1992.
5. Manuals from Xilinx, Altera, AMD, Actel.

EC 5106

VLSI TECHNOLOGY

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction – Integrated Circuits Review of history of VLSI technology progress–. Electronic Functions – Components – Analog and Digital ICs. Basic Devices in ICs – Structures Resistors – Capacitors – Inductors. Diodes – Bipolar Junction Transistors – Field Effect Transistors. Isolation techniques in MOS and bipolar technologies.

UNIT – II

Monolithic ICs – Silicon as the Base Material and its advantages, various Layers of ICs – Substrate – Active Layer -Oxide/Nitride Layers – Metal/Poly Silicon Layers – Functions of Each of the Layers. Process Flow for Realization of Devices. Description of Process Flow for Typical Devices viz., FET and BJT.

UNIT – III

Silicon Wafer Preparation – Electronic Grade Silicon – CZ and FZ Methods of Single Crystal Growth – Silicon Shaping – Mechanical Operations, Chemical Operations – Prefabrication Processes.

Epitaxy: Growth Dynamics – Process Steps. Vapour phase, Solid phase and Molecular Beam Epitaxial Processes. Epitaxial Reactors.

Oxide Growth: Structure of SiO_2, Growth Mechanism and Dynamics – Oxide Growth by Thermal method.

UNIT – IV

Deposition techniques Chemical Vapour Deposition (CVD) and associated methods like LPCVD and PECVD. PVD thermal evaporation and sputtering. Step coverage issues.

Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their characteristics, optical exposure systems contact and projection systems, steppers, X-ray – Electron Beam Lithography.

Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT – V

Ion implantation: Range and Penetration Depth – Damage and Annealing – Ion Implantation machine.

Diffusion: Constant and Infinite Source Diffusions – Diffusion Profiles – Diffusion Systems – Multiple Diffusions and Junction Formations. Packaging: die and Bonding and Packaging, Testing. Clean rooms and their importance in VLSI technology

Suggested Reading:

1. S.M. Sze, VLSI Technology, Mc Grawhill International Editions.
2. CY Chang and S.M. SZe , VLSI Technology, Tata Mc Graw-Hill Companies Inc.
3. J.D. Plummer, M.D. Deal and P.B. Griffin ,The Silicon VLSI Technology Fundamentals, Practice and modeling, Pearson Education 2009
4. Stephen A, The Science and Engineering of Microelectronic Fabrication, Campbell Oxford 2001.

EC 5110

MEMS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT – II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Deflection, Description of the above wrt. Fixed Beams. Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT – III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications

UNIT – IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT – V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

Suggested Reading:

1. Gabriel.M. Reviez, R.F. MEMS Theory, Design and Technology, Thon Wiley & Sons, 2003.
2. Thimo Shenko, Strength of Materials, CBS Publishers & Distributors.
3. K. Pitt, M.R. Haskard, Thick Film Technology and Applications, 1997.
4. Wise K.D. (Guest Editor), “Special Issue of Proceedings of IEEE”, Vol.86, No.8, Aug 1998.
5. Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994.

EC 5111

INTEGRATED OPTICS & PHOTONIC SYSTEMS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT - I

Introduction, advantages, comparison of optical IC with electrical IC, applications of integrated optics, substrate materials for optical IC. Optical wave guide mode, modes in a planar wave guide, ray optic approach to optical mode theory, basic three layer waveguide, symmetric and asymmetric wave guide, rectangular channel and strip loaded wave guides. Wave guide fabrication technique, deposited thin film, substitution dopant atoms, carrier concentration reduction wave guide, epitaxial growth, electro optic wave guide.

UNIT - II

Polymer and fiber integrated optics, polymer processing, applications, polymer wave guide devices, optical fiber wave guide devices, fiber sensor, types, applications. Losses in optical wave guide, measurement of losses. Wave guide input and output couplers, types of couplers, coupling between wave guides, coupled mode theory, wave guide modulator,

UNIT - III

Electro optic modulator, single and dual channel electro optic modulator acousto optic modulator. Integrated semiconductor laser, integrated semiconductor optical amplifier, monolithical integrated direct modulator, direct modulation of QD laser, integrated optical detectors, structures, factors affecting the performance, principle of micro optical devices.

UNIT – IV

Optical amplifiers, semiconductor laser amplifier, doped fiber amplifiers, Fiber Raman amplifier, fiber Brillouin amplifier, noise characteristics ,crosstalk, system applications. Direct detection light wave system, digital optical receiver, direct detection with optical amplifiers, performance.

UNIT - V

Coherent detection light wave system, system configurations, performance. Soliton light wave system,soliton wave propagation, soliton amplification, system design.

Suggested Reading:

1. Robert Hunsperger, *Integrated optics :Theory and technology* 6/e Springer, 2009
2. Keico Iizuka, *Elements of photonics*, John Wiley, 2002
3. Pappannareddy, *Introduction to light wave systems*,Artech House,1995
4. Lifante, *Integrated Photonics: Fundamentals* ,John Wiley 2003

EC 5112

RFIC DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT – II

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT – III

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT – IV

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT – V

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

Suggested Reading:

1. BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.
3. B. Leunge, VLSI for Wireless Communication, Personal Education Electronics and VLSI series, Pearson Education, 2002.

EC 5113

HIGH LEVEL SYNTHESIS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction to C-based FPGA Design , Using Vivado HLS HLS UltraFast Design Methodology Managing Interfaces Design Optimization RTL Verification, Exporting the RTL Design

UNIT – II

Introduction to the Vivado HLS C Libraries, Arbitrary Precision Data Types Library, The HLS Stream Library, HLS Math Library, Vivado HLS Video Library, The HLS IP Libraries, HLS Linear Algebra Library.

UNIT – III

Coding Styles: Unsupported C Constructs, The C Test Bench Functions, Loops, Arrays, Data Types. C++ Classes and Templates, Using Assertions, SystemC Synthesis.

UNIT – IV

Command Reference, Graphical User Interface (GUI) Reference, Send Feedback, Interface Synthesis Reference, AXI4 Slave Lite C Driver Reference, Video Functions Reference.

UNIT – V

HLS Linear Algebra Library, C Arbitrary Precision Types, C++ Arbitrary Precision Types, C++ Arbitrary Precision Fixed Point Types, Comparison of SystemC and Vivado HLS Types.

Suggested Reading:

1. Andres Takach, Creating C++ IP for High Performance Hardware Implementations of FFTs. DesignsDesignCon2002.
2. Preston A. Jackson, Cy P. Chan, Jonathan E. Scalera, Charles M. Rader, and M. Michael Vai - A Systolic FFT Architecture for Real Time FPGA Systems. MIT Lincoln Laboratory 244 Wood ST, Lexington, MA 02420
3. Vivado Design Suite User Guide and Vivado Design Suite Tutorial for High-Level Synthesis.

EC 5200

SYSTEM ON CHIP ARCHITECTURE

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor, Processor design trade off, Design for low power consumption. ARM Processor as System-on-Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface.

UNIT – II

ARM Assembly Language Programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions. Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

UNIT – III

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design- an example – memory management.

Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

UNIT – IV

Architectural Support for Operating System: An introduction to Operating Systems – ARM System control coprocessor – CP15 protection unit registers – ARM protection unit – CP15

MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output.

UNIT – V

System in Package Design: Advantages and disadvantages between SoC, SiC and board level design; SiP Design flow, System Planning, Chip-Package co-design, System Optimization; SiP Design Layout, Simulation, Verification; Gaps in SiP Design, Power optimization tools, Parasitic extraction tools, Signal Integrity.

Examples of SiP.

Suggested Reading:

1. Steve Furber, ARM System on Chip Architecture, 2nd ed., Addison Wesley Professional, 2000.
2. Ricardo Reis, Design of System on a Chip: Devices and Components, 1st ed., Springer, 2004.
3. Jason Andrews, Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) , BK and CDROM.
4. Prakash Rashinkar, System on Chip Verification – Methodologies and Techniques, Peter Paterson and Leena Singh L ,Kluwer Academic Publishers, 2001.
5. System in Package (SiP) – A review, Technical Review-I, R&D Cell, Vasavi College of Engineering, Ibrahimbagh, Hyderabad, Telangana.

EC 5201

SCRIPTING LANGUAGES FOR EMBEDDED SYSTEMS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Overview of scripting languages-PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT – II

Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT – III

Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions.
Inter process communication,- signals, files, pipes, sockets,.

UNIT – IV

Threads- process model, thread model, Perl debugger- using debugger commands, customization, internals and externals, internal data types, extending Perl, embedding Perl, exercises for programming using Perl.

UNIT – V

Other languages: Broad features of other scripting languages SKILL, CGI, java script, VB script.

Suggested Reading:

1. Larry Wall, Tom Christiansen, John Orwant, “programming perl”, oreilly publications, 3rd edition.
2. Randal L, Schwartz Tom Phoenix, “Learning PERL”, Oreilly publications.

EC 5202

INTERNET OF THINGS

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

M2M to IoT: The Vision-Introduction, From M2M to IoT, M2M towards IoT-the global context, A use case example, Differing Characteristics.

UNIT – II

M2M to IoT – A Market Perspective: Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT – III

M2M and IoT Technology Fundamentals: Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service(XaaS), M2M and IoT Analytics, Knowledge Management

UNIT – IV

IoT Architecture-State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model

UNIT – V

IoT Reference Architecture: Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints-hardware is popular again, Data representation and visualization, Interaction and remote control. Industrial Automation- Service-oriented architecture-based device integration, SOCRADES: realizing the enterprise integrated Web of Things, IMC-AESOP: from the Web of Things to the Cloud of Things, Commercial Building Automation- Introduction, Case study: phase one-commercial building automation today, Case study: phase two- commercial building automation in the future.

Suggested Reading:

1. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2014.
2. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1stEdition, VPT, 2014.
3. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.

EC 5203

GRAPH THEORY & ITS APPLICATIONS TO VLSI

Instruction	3 Periods per week	External Examination – Duration	3 Hours
Sessionals	30 Marks	External Examination – Marks	70 Marks
Credits	03		

UNIT – I

Introduction: Basic definitions, results and examples relating to Graph theory, self-complementing graphs and properties of graphs, Trees, Spanning tree & directed graphs.

UNIT – II

Definitions of strongly, weakly, unilaterally connected graphs and deadlocks. Metric representation of graphs. Classes of graphs: standard results relating to characterization of Hamiltonian graphs, standard theorems

UNIT – III

Self-centered graphs and related theorems. Chromatic number vertex and edge – application to coloring, linear graphs, Euler's formula.

UNIT – IV

Graph algorithms: DFS – BFS algorithms, min. spanning tree and max. spanning tree algorithm. Directed graphs algorithms for matching, properties flow in graph and algorithms for max flow. PERT-CPM, complexity of algorithms, P-NP – NPC – NP hard problems and examples.

UNIT – V

Linear integer and dynamic programming: Conversions of TSP, max. flow, shortest path problems. Branch bound methods, critical path and linear programming conversion. Floor shop scheduling problem, personal assignment problem, dynamic programming - TSP – best investment problems.

Suggested Reading:

1. C. Papadimitriou & K. Steiglitz, Combinational Optimization Prentice Hall, 1982.
2. H. Gerej, Algorithms for VLSI Design Automation, John Wiley, 1992.
3. B. Korte & J. Vygen, Combinational Optimization, Springer Verilog, 2000.
4. G.L. Nemhauser & AL Wolsey, Integer & Combinatorial Optimization, John Wiley,1999.
5. W.J. Cook et al, "Combinational optimization", John Wiley,2000.

EC 5204

SYSTEM DESIGN AND RELIABILITY

Instruction	3 Periods per week	External Examination – Duration	3 Hours
Sessionals	30 Marks	External Examination – Marks	70 Marks
Credits	03		

UNIT – I

System design aspects- Structure of systems in general-hardware, software components, testability of systems, and design of systems from testability point of view.

UNIT – II

System Reliability: Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces. Test environments, testing for reliability and durability, failure reporting,

UNIT – III

Concepts of MTBF Maintainability and Availability. Maintainability and its equation. Factors Affecting maintainability. Measures of, Maintainability, Mean Down Time, Availability Intrinsic availability equipment availability & Mission availability. Replacement processes and Policies.

UNIT – IV

Reliability of electronic components, component types and failure mechanisms,: Evaluation of reliability of electronic components like integrated circuits. Life cycle of electronic components, bath tub curve. Accelerated life tests for components, reliability screening procedures, burn in test. Standards for reliability evaluation and screening at component level.

UNIT – V

System level reliability testing, - Reliability evaluation and screening procedures at system level. Life tests for systems, accelerated testing reliability costs, Standards for system level reliability evaluation and screening.

Suggested Reading:

1. Kailash C. Kapur, Michael Pecht, Reliability Engineering, Wiley, 2014.
2. Patrick D.T. O' Connor, David Newton and Richard Bromley, Practical Reliability Engineering, 4/e , John Wiley & Sons, 2002.
3. Elmer Eugene Lewis, Introduction to Reliability Engineering, 2/e, Wiley International, 1996.

EC 5205

HARDWARE – SOFTWARE Co-DESIGN

Instruction	3 Periods per week	External Examination – Duration	3 Hours
Sessionals	30 Marks	External Examination – Marks	70 Marks
Credits	03		

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages, Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Suggested Reading:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

EC 5206

ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

Instruction	3 Periods per week	External Examination – Duration	3 Hours
Sessionals	30 Marks	External Examination – Marks	70 Marks
Credits	03		

UNIT – I

Introduction and Sources of EMI: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT – II

Types of Electromagnetic Coupling:Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near78 Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT – III

EMI Measurements: EMI Shielded Chamber, Open Area Test Site, TEM Cell, GTEM cell Sensors/ Injectors/ Couplers, LISN, voltage probe, Current probe Test beds for ESD and EFT.

UNIT – IV

EMI Mitigation Techniques: Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT – V

EMC System Design: PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Suggested Reading:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996
2. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", 2nd Edition, John Wiley and Sons, NewYork. 1988.
3. C.R.Paul, "Introduction to Electromagnetic Compatibility", John Wiley and Sons, Inc, 2006.
4. Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.

EC 5210

DESIGN OF FAULT TOLERANT SYSTEMS

Instruction	3 Periods per week	External Examination – Duration	3 Hours
Sessionals	30 Marks	External Examination – Marks	70 Marks
Credits	03		

UNIT – I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT – II

Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT – III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT – IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT – V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

Suggested Reading:

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI.
2. Digital System Test and Testable Design using HDL models and Architectures -Zainalabedin Navabi, Springer International Edition.
3. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books.
4. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal, Springers.
5. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008, Pearson Education.

EC 5211

RECONFIGURABLE SYSTEM DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT - I

Introduction: Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

UNIT - II

Parallel and Advanced Processors: Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

UNIT - III

Reconfigurable Architectures: FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

UNIT - IV

Reconfiguration Management : Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time

UNIT - V

Case Studies of FPGA Applications: Dynamic Partial Reconfigurable FIR Filter Design, Trigonometric Computing, Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip, A Fast Run Time Reconfigurable Platform for Image Edge Detection, Efficient Floating-Point Implementation of High-Order (N) LMS Adaptive Filters in FPGA, Area/Performance Improvement of NoC Architectures.

Suggested Reading:

1. Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer 2007
2. Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA based Computation”, Elseiver 2008
3. Niccolo Battezzatti, Luca Sterpone, Massimo Violante, “Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications”, Springer 2011.
4. Kai Hwang, “Advanced computer architecture – Parallelism, Scalability, Programmability”; Tata McGraw Hill Publishing company Ltd., New Delhi, 1993.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, “Reconfigurable Computing: Architectures and Applications”, Springer 2006.

EC 5211

SOFT COMPUTING TECHNIQUES

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Fundamentals of Neural Networks & Feed Forward Networks: Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Single Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II

Associative Memories & ART Neural Networks: Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III

Fuzzy Logic & Systems: Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV

Genetic Algorithms : Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V

Hybrid Systems: Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

Suggested Reading:

1. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
2. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
3. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi, 1994.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998.

EC 5213

LOW POWER EMBEDDED SYSTEMS DESIGN

Instruction	3 Periods per week	External Examination - Duration	3 Hours
Sessionals	30 Marks	External Examination - Marks	70 Marks
Credits	03		

UNIT – I

Setting-up the software – tool chain. Setting-up the hardware – microcontroller master clock, basic Input/Output (I/O) techniques.

UNIT – II

Basic serial communication, serial communications using interrupts, analogue to digital conversion (ADC).

UNIT – III

Creating precise timing using timers. Interfacing to a liquid crystal display (LCD).

UNIT – IV

Accurately measuring time interval between input events – interrupts generated from input transitions and use of timers. Processor low power and sleep modes.

UNIT – V

Case studies for two applications followed by a mini project.

Suggested Reading:

1. Esin Terzioglu, et al, “Low Power Embedded Memory Design - Process to System Level Considerations”.
2. Jong Wook Kwak; Ju Hee Choi; " Selective Access to Filter Cache for Low-Power Embedded Systems" 43rd Hawaii International Conference on System Sciences (HICSS).
3. A. Asaduzzaman, F.N.Sibai “Investigating Cache Parameters and Locking in Predictable and Low Power Embedded Systems”, 22nd International Conference on Microelectronics.
4. T.S. Rajesh Kumar, C.P. Ravikumar, R. Govindarajan “Memory Architecture Exploration Framework for Cache Based Embedded SoC”, 21st International Conference on VLSI Design.