VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

Accredited by NAAC with 'A++' Grade
Ibrahimbagh, Hyderabad-31
Approved by A.I.C.T.E., New Delhi and
Affiliated to Osmania University, Hyderabad-07

Sponsored
by
VASAVI ACADEMY OF EDUCATION
Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR M.E. (ECE)

EMBEDDED SYSTEMS AND VLSI DESIGN

(ES&VLSID)

I TO IV SEMESTERS

With effect from 2021-23
(For the batch admitted in 2021-22)
(R-21)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Phones: +91-40-23146040, 23146041
Fax: +91-40-23146090

Institute Vision

Striving for a symbiosis of technological excellence and human values

Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering

Department Mission

To inculcate a spirit of scientific temper and analytical thinking, and train the students in contemporary technologies in Electronics & Communication Engineering to meet the needs of the industry and society with ethical values.

Program Educational Objectives (PEO) :

PG – M.E (ES & VLSID) : Embedded Systems and VLSI Design

PEO1: Graduates will be able to acquire indepth knowledge in the field of Embedded Systems and VLSI Design for designing and implementing systems employing latest techniques and tools

PEO2: Graduates will be able to carry out research independently and write & present a substantial research report

PEO3: Graduates will be able to demonstrate effective communication skills and leadership qualities with ethical attitudes in broad societal context while working in a multiple disciplinary environment

Program Outcomes (PO) :

PG – M.E (ES & VLSID) : Embedded Systems and VLSI Design :
Graduates will have

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: An ability to demonstrate a degree of mastery over the area of Embedded Systems and VLSI Design.

PO4: An ability to apply appropriate techniques and modern engineering tools in the design and implementation of VLSI and Embedded Systems.

PO5: An ability to apply engineering and Management principles as a member and leader in a team, to manage projects in multi-disciplinary environment with lifelong learning capabilities

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

DEPARTMENTOF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION FOR

M.E - ECE (ES&VLSID) EMBEDDED SYSTEMS AND VLSI DESIGN

I-SEMESTER under CBCS Scheme for 2021-22 Batch **(R - 21)**

M.E - ECE (ES&VLSID) I-Semester									
S.No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
			Hours per Week			Duration in Hrs	Maximum Marks		Credits
			L	T	P/D		SEE	CIE	
THEORY									
1	PI21PC110EC	PC-I : Embedded System Design	3	-	-	3	60	40	3
2	PI21PC120EC	PC-II : Digital IC Design	3	-	-	3	60	40	3
3	PI21PC130EC	PC-III : Analog IC Design	3	-	-	3	60	40	3
4	PI21PE1X0EC	Professional Elective – I	3	-	-	3	60	40	3
5	PI21PE1X0EC	Professional Elective - II	3	-	-	3	60	40	3
6	PI21HS110EH	Skill Development Course-I: Communication Skills	1	-	-	2	40	30	1
7	PI21PE170EC	Skill Development Course -II: Technical Skills – I	2	-	-	3	60	40	2
8	PI21AC110EH	AC-I : English for Research Paper Writing	2	-	-	3	60	40	-
LABORATORY									
9	PI21PC111EC	Embedded Systems Laboratory	-	-	3	-	-	50	1.5
10	PI21PC121EC	Design and Simulation Laboratory - I	-	-	3	-	-	50	1.5
11	PI21PC138EC	Seminar	-	-	2	-	-	50	1
		Total	**20**	**-**	**8**	**-**	**460**	**460**	**22**
		Grand Total	**28**				**920**		
Left over hours will be allocated for : Library/ Proctorial Interaction / FC /CCA									
Note: Every student should acquire one online course certification equivalent to 2 Credits weightage during I to III Semester									

S. No.	Course Code	Course	Hours per week
Professional Core Courses (R – 21)			
1	PI21PC110EC	Core – I: Embedded System Design	3
2	PI21PC120EC	Core – II: Digital IC Design	3
3	PI21PC130EC	Core – III: Analog IC Design	3
4	PI21PC210EC	Core – IV: Embedded Real Time Operating Systems	3
5	PI21PC220EC	Core – V: Mixed Signal IC Design	3
6	PI21PC230EC	Core – VI: VLSI Physical Design	3
7	PI21PC111EC	Embedded Systems Laboratory	3
8	PI21PC121EC	Design and Simulation Laboratory-I	3
9	PI21PC138EC	Seminar	2
10	PI21PC240ME	Research Methodology and IPR	2
11	PI21PC211EC	Embedded Systems Application Laboratory	3
12	PI21PC221EC	Design and Simulation Laboratory –II	3
13	PI21PW219EC	Mini Project	2
14	PI21HS110EH	Skill Development Course -I : Communication Skills	1
15	PI21HS210EH	Skill Development Course -III : Aptitude	1
16	PI21PW319EC	Dissertation-Phase-I / Internship	8
17	PI21PW419EC	Dissertation-Phase-II / Internship	20

S. No.	Course Code	Course	Hours per week
Professional Electives (R – 21)			
Elective – I			
1	PI21PE110EC	Advanced Computer Organization	3
2	PI21PE120EC	Programming Languages for Embedded Software	3
3	PI21PE130EC	IoT Architectures and Protocols	3
Elective – II			
4	PI21PE140EC	VLSI Technology	3
5	PI21PE150EC	Hardware Descriptive Languages	3
6	PI21PE160EC	Design and Verification using System Verilog	3
Elective – III			
7	PI21PE210EC	Low Power VLSI Design	3
8	PI21PE220EC	Hardware-Software Co-design	3
9	PI21PE230EC	CPLD & FPGA Architectures and Applications	3
Elective – IV			
10	PI21PE310EC	Physical Design Automation	3
11	PI21PE320EC	High Level Synthesis	3
12	PI21PE330EC	System on Chip (SoC) Design	3
Elective – V			
13	PI21PE340EC	Design for Testability	3
14	PI21PE350EC	Scripting Languages	3
15	PI21PE360EC	Static Timing Analysis	3
Technical Skills			
16	PI21PE170EC	Skill Development Course -II: Technical Skills – I	2
17	PI21PE240EC	Skill Development Course -IV: Technical Skills - II	2

S. No.	Course Code	Course	Hours per week
Audit Course – I (R – 21)			
1	PI21AC110EH	English for Research Paper Writing	2
2	PI21AC120XX	Value Education	2
3	PI21AC130XX	Stress Management by Yoga	2
4	PI21AC140XX	Sanskrit for Technical Knowledge	2
Audit Course –II			
1	PI21AC210EH	Pedagogy Studies	2
2	PI21AC220XX	Personality Development through Life Enlightenment Skills	2
3	PI21AC230XX	Constitution of India	2
4	PI21AC240XX	Disaster Management	2
Open Electives			
1	PX21OE310CS	Fundamentals of Python Programming	3
2	PX21OE320XX	Industrial Safety	3
3	PX21OE330ME	Advanced Operations Research	3
4	PX21OE340XX	Cost Management of Engineering Projects	3
5	PX21OE350XX	Composite Materials	3
6	PX21OE360XX	Waste to Energy	3
7	PX21OE370XX	Business Analytics	3

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded System Design

Professional Core - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC110EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Implement embedded hardware & firmware using embedded-C for C51 to interface with different I/O. 2. Demonstrate the embedded system design using ARM IP core with emphasis on its programming model. 3. Interpret serial and parallel bus communication protocols used for providing connectivity and propose debugging techniques for testing.	On completion of the course, students will be able to 1. Define, Classify and Analyze embedded system product design with IC Technology. 2. Design & implement device drivers in embedded-C for C51 target MCU to interface I/O. 3. Analyze ARM IP Core usage in design with its programming model. 4. Justify the hardware software co-design issues along with debugging techniques. 5. Propose serial & parallel protocols to design networked embedded systems.

UNIT – I

Embedded Systems Overview: Definition of Embedded System; Examples; Design Challenges–Optimizing Design Metrics; Selection of processor or controller & memories; Processor Technology; RISC Vs CISC

UNIT – II

Real World Interfacing using Embedded C with AT89S52 (8051 Microcontroller): ADC0808, LED, Seven Segment Displays, DAC, LCD, Keypad, RTC, DC Motor, Stepper Motor driving actuators using PWM.

UNIT – III

ARM Core Architecture: Introduction to RISC concepts with ARM as CPU, ARM engine Architecture, AMBA Bus, Core Registers, Programming Modes, Importance of Thumb Mode, CPSR, SPSR, Pipeline, Exceptions, Interrupts

and vector table; ARM Programming Model; Core Extensions, ARM Revisions, ARM processor families and comparisons.

UNIT – IV

Embedded Networking: Serial protocols topology & working principles and frame formats – I^2C; SPI; USB; CAN; Ethernet; Parallel Protocols – PCI; PCIx; AMBA bus

UNIT – V

Embedded Debugging Techniques: Debugging Methods using Software and Hardware; usage of JTAG adaptor for ARM and Embedded ICE Embedded Software Architectures Introduction: Round-Robin; RR with Interrupt; Functional Queue Scheduling & need of RTOS

Learning Resources:

1. Frank Vahid, Tony Givargis "Embedded System Design – A Unified Hardware/Software Introduction" John Wiley & Sons, Inc. 2002.
2. Andrew N Sloss, Dominic Symes & Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", The Morgan Kaufmann Series 2004.
3. Mazidi M.A and Mazidi J.G, "The 8051 Microcontroller and Embedded Systems", Pearson 2007.
4. David E Simon, "An Embedded Software Primer", Pearson Education, 2005.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Digital IC Design

Professional Core - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC120EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Appreciate the importance of secondary effects such as velocity saturation, sub-threshold leakage of MOSFETS and study the modifications in the device models in DSM regime. 2. Analyse the effect of sizing the devices on CMOS inverter performance the inverters, 3. Optimize critical data paths considering Logical, Electrical and Branch Efforts 4. Estimate power and delay in both static and dynamic CMOS combinational and sequential circuits 5. Design arithmetic building blocks and memory blocks for use in a microprocessor and analyse their performance.	On completion of the course, students will be able to 1. Appreciate the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay, 2. Perform path optimization of CMOS gates with Logical Effort, 3. Compute delay and power dissipation in both dynamic and static CMOS designs, and apply pipelining techniques to optimize Sequential Circuits 4. Analyse the interconnect parasitics and their effect on clock distribution 5. Design a simple datapath for a processor and apply power reduction techniques 6. Design a 6T SRAM cell and organise a memory bank

UNIT – I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, MOSFET secondary effects, Simple Interconnect Wire models, Design rules, Sub-threshold Conduction. CMOS Inverter – Static and Dynamic Behaviour, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis, Detailed Load Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

UNIT – II

Designing Combinational Logic in CMOS: Static CMOS design: Complimentary CMOS, Ratioed Logic, Pass Transistor Logic, Transmission Gate Logic, Optimizing Paths with Logical effort.

Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic, Signal Integrity Issues, Cascading Dynamic Gates

UNIT – III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles, Pipelining to optimize Sequential Circuits, Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic, Advanced Interconnect Techniques, Power Grid and Clock design: Power Distribution Design, Clocking and Timing Issues, Phase-Locked Loops / Delay Locked Loops.

UNIT – IV

Designing Arithmetic Building Blocks: Datapaths in Digital Processor Architectures,: The Adder, The Multiplier, The Shifter and The Comparator. Power and Speed Trade offs in Datapath Operators: Design-Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues

UNIT – V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, SRAM Cell Layout

Learning Resources:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective"", Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in DSM Technology", 3rd Edition, Tata McGraw Hill, 2008.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
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Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Analog IC Design

Professional Core - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC130EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Realize that ICs are similar to discrete component circuits with special constraints. 2. aexposed to these constraints and make them design the ICs. 3. Capable of arriving at a suitable architecture, for a given function, which can be realized in IC form	On completion of the course, students will be able to 1. Apply mathematics and physics to model analog circuits. 2. Arrive at an optimum solution to a problem in analog circuits domain. 3. Design simple CMOS analog circuits and analyse of their performance 4. Design and analyse the performance of Operational amplifiers

UNIT – I

Introduction: What are electronic devices and circuits – Types of electrical signals – Characteristics of analog signals – Analog functions – Devices characteristics needed to perform these functions. Discrete component approach to analog circuit – Integrated circuit approach, silicon as base material. Integrated circuit – Components for Ics – Resistors, Capacitors, inductors diodes, BJTS, MOSFETS – Their IC architectures, limitations, circuits design philosophies – Different families of circuits device models. Basic analog circuits – Amplifiers – Different type of loads – Biasing techniques – current mirrors – Coupling techniques between stages.

UNIT – II

Biasing techniques: Basic current mirror architecture – Specifications of current mirrors – Cascode current mirrors – Wide swing current mirrors Wilson current mirror – Degenerate current sources – peaking current sources for very low current biasing – enhanced output impedance current mirrors, Sensitivity analysis of current. Mirrors: Voltage references – VBE, VT and Zenner diode based references, Band gap reference

UNIT – III

Single stage amplifiers CS, CG, CD amplifiers with resistive, diode, current source, and current mirror loads – performance analysis of these circuits – input, output, current and voltage gains at low frequencies swing, frequency response and phase response of these amplifiers, Multistage amplifiers and biasing and swing problems. Cascode amplifiers – Folded cascade amplifiers – Swing analysis. Differential amplifiers, biasing and analysis of performance, Specifications – common and differential mode gain – common mode rejection ratio power rejection ratio, swing differential input differential output amplifier, differential input single ended output amplifier variable gain amplifiers Noise in amplifiers.

UNIT – IV

Operational amplifiers – characteristics and specifications – Two and three stage Op-Amps – analysis of gain, frequency and phase response – Coupling problems, fully differential amplifiers – Cacodes, folded 11ascades – common mode feedback, and circuits, active cascade Op-Amp – current differential amplifiers – current feedback Op-Amps, - Gilbert Cells. OTAS.

UNIT – V

Oscillators and mixers: Basics of oscillators – Feedback oscillators, negative resistance oscillators, (two port oscillators), ring oscillators – Differential ring oscillators, LC oscillators, relaxation oscillators, voltage controlled oscillators, Tuning delay and frequency. Diode based mixers, Gilbert cell based mixers.

Learning Resources:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Computer Organization

Professional Elective - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE110EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Advanced computing/processing system includes several functional aspects like processing, memory, high speed logic, industry standard interfaces and so on. The major objective of this course is to combine all these functional aspects and develop a processing system for the given specifications.	On completion of the course, students will be able to 1. Evaluate the performance parameters of advanced processors, analyse and compare advantages, limitations and applications of advanced processors. 2. Design the data path and control unit for the given specifications and analyze different control unit design approaches. 3. Demonstrate the knowledge of issues involved in memory organization. 4. Analyze various input-output techniques for proper transfer of data between CPU and different peripheral devices. 5. Use modern EDA tools for solving advanced processing system related problems. 6. Become acquainted with recent advancements in the area of advanced processing systems.

UNIT – I

Review of Computer Arithmetic, Application Processing Unit, A Note on the ARM Model, Standard Processor and processing system, Processor Design Techniques: Instruction Pipelining, Super Scalar techniques, Super scalar and super pipeline design, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

UNIT – II

Control Unit Design approaches, Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Processor Selection Criteria, Case studies on MicroBlaze Processor, Discrete FPGA-Processor

UNIT – III

Memory Organization: the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT – IV

I-O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Synchronous bus and asynchronous bus, IO Processor, General Purpose Input/Output ,Communications Interfaces,Programmable Logic Interfaces, AXI Standard, AXI Interconnects and Interfaces, Processing System External Interfaces

UNIT – V

Parallel Computer Systems: Instruction Level Parallelism (ILP) , Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors, SIMD computers and Super computers, High Performance Computing(HPC), Case study on advanced processing system, An Overview of HPC Applications

Learning Resources:

1. William Stallings, Computer Organization and Architecture designing for Performance, 7th edition, PHI, 2007.
2. Carl Hamacher, Vranesic, Zaky, Computer Organization, 5th edition, MGH.
3. Hayes John P; Computer Architecture and organization; 3rd Edition, MGH, 1998.
4. John L. Hennessy and David A. Patterson, Computer Architecture – A quantitative Approach, 3rd Edition, Elsevier, 2005.
5. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Programming Languages for Embedded Software

Professional Elective - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE120EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To impart knowledge on embedded C	On completion of the course, students will be able to 1. Write an embedded C application of moderate complexity. 2. Develop and analyze algorithms in C++. 3. Differentiate interpreted languages from compiled languages. 4. Explain various templates

UNIT – I

Embedded 'C' Programming
- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT – II

Object Oriented Programming - Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT – III

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT - IV

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT – V

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Learning Resources:

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011
3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

IoT Architectures and Protocols

Professional Elective - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE130EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. The purpose of this course is to impart knowledge on IoT Architecture, practical constrains. 2. To study various protocols And to study their implementations	On completion of the course, students will be able to 1. Understand the Architectural Overview of IoT 2. Enumerate the need and the challenges in Real World Design Constraints 3. Choose the required protocol for a particular application. 4. Compare the various IoT Protocols (Datalink, Network, Transport, Session, Service) 5. Understand IoT usage in various applications

UNIT - I : OVERVIEW

IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT.

UNIT - II : REFERENCE ARCHITECTURE

IoT Architecture-State of the Art – Introduction, State of the art, Reference Model and architecture, IoT reference Model - IoT Reference Architecture Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints-hardware is popular again, Data representation and visualization, Interaction and remote control.

UNIT - III : IOT DATA LINK LAYER & NETWORK LAYER PROTOCOLS

PHY/MAC Layer(3GPP MTC, IEEE 802.11, IEEE 802.15), Wireless HART,Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-IPv4, IPv6, 6LoWPAN, 6TiSCH,ND, DHCP, ICMP, RPL, CORPL, CARP.

UNIT - IV : TRANSPORT, SESSION LAYER, SERVICE LAYER PROTOCOLS & SECURITY PROTOCOLS

Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT.

Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC 802.15.4, 6LoWPAN, RPL, Application Layer.

UNIT - V : IoT case studies

Smart Cities and Smart Homes, Connected Vehicles, Agriculture, Healthcare, Activity Monitoring.

Learning Resources:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1 st Edition, Academic Press, 2014.
2. Peter Waher, "Learning Internet of Things", PACKT publishing, BIRMINGHAM – MUMBAI
3. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer
4. Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118- 47347-4, Willy Publications.
5. https://nptel.ac.in/courses/106105166/5
6. https://nptel.ac.in/courses/108108098/4

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Technology

Professional Elective - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE140EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Impart a knowledge about VLSI Integrated circuits their structures, evolution and benefits of these circuits in realizing complex electronics functions to students. 2. Impart knowledge about IC fabrication technologies and their advancement over time. 3. Impart knowledge about the sub process technologies that are involved in IC fabrication and how they are put together to form complete fabrication process. 4. Acquaint the students about clean room environments needed for IC fabrication and their importance. 5. Impart knowledge about complex process of VLSI packaging and testing and their advancements.	On completion of the course, students will be able to 1. Describe evolution and progress of VLSI technology, Electronic functions and basic device structures on Integrated circuits. 2. Apply alternate technologies and Process flows for realization of VLSI chips 3. Demonstrate Unit processes involved in VLSI technology such as silicon wafer preparation, epitaxy, oxidation and diffusion, lithography, etching, implantation etc. 4. Specify Other unit processes involved in VLSI technology such as deposition, lithography and etching 5. Specify Clean Room environments needed for VLSI processing and packaging and testing of the VLSI chips.

UNIT – I

Introduction – Integrated Circuits Review of history of VLSI technology progress–. Electronic Functions – Components – Differences between - Analog and Digital ICs. Basic Devices in ICs – Structures Resistors – Capacitors – Inductors. Diodes – Bipolar Junction Transistors – Field Effect Transistors. Isolation techniques in MOS and bipolar technologies.

UNIT – II

Monolithic ICs – Silicon as the Base Material and its advantages, various Layers of ICs – Substrate – Active Layer -Oxide/Nitride Layers –

Metal/Poly Silicon Layers – Functions of Each of the Layers. Description of Process Flow for Typical Devices viz., FET and BJT.

UNIT – III

Silicon Wafer Preparation – Electronic Grade Silicon – CZ and FZ Methods of Single Crystal Growth – Silicon Shaping – Mechanical Operations, Chemical Operations – Prefabrication Processes.

Epitaxy: Growth Dynamics – Process Steps. Vapour phase, Solid phase and Molecular Beam Epitaxial Processes.

Oxide Growth: Structure of SiO_2, – Oxide Growth by Thermal method.

UNIT – IV

Deposition techniques Chemical Vapour Deposition (CVD) and associated methods like LPCVD and PECVD. PVD thermal evaporation and sputtering. Step coverage issues.

Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their characteristics, steppers, X-ray – Electron Beam Lithography.

Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT – V

Ion implantation: Range and Penetration Depth – Damage and Annealing. Diffusion: Constant and Infinite Source Diffusions – Diffusion Profiles – Multiple Diffusions and Junction Formations. Packaging: Bonding and Packaging, Testing. Clean rooms and their importance in VLSI technology

Learning Resources:

1. S.M. Sze, VLSI Technology, Mc Grawhill International Editions.
2. CY Chang and S.M. SZe , VLSI Technology, Tata Mc Graw-Hill Companies Inc.
3. J.D. Plummer, M.D. Deal and P.B. Griffin ,The Silicon VLSI Technology Fundamentals, Practice and modeling, Pearson Education 2009
4. Stephen A, The Science and Engineering of Microelectronic Fabrication, Campbell Oxford 2001.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Hardware Descriptive Languages

Professional Elective - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE150EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

Course Objectives	Course Outcomes
To impart knowledge on Hardware descriptive Languages	On completion of the course, students will be able to 1. Differentiate sequential and concurrent languages 2. Design combinational logic circuits using HDL. 3. Design sequential logic circuits using HDL. 4. Model Analog circuits using Verilog AMS.

UNIT - I

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator overloading

UNIT - II

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To
Design Combinational Circuits

UNIT - III

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to One Hot

UNIT - IV

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators,

UNIT - V

Applications of Verilog-AMS, Analog Modeling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

Learning Resources:

1. Volnei A. Pedroni, Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press, 2010.
2. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design and Verification using System Verilog

Professional Elective - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE160EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Students will build a layered test bench and simulate a simple ligic block 2 They will learn the important features of System Verilig 3 They will develop a test bench using object oriented concepts for veryfying a digital system 4 They will understand the limitations of Randomization of functions and implement random device configuration 5 They will connect the test bench and design of a given system	On completion of the course, students will be able to 1 Identify the need for a test bench and specify the formal verification techniques (PO2) 2 Implement simulation based verification of a given system (PO2) 3 Implement a formal test bench using object oriented concepts for veryfying a digital system. (PO3) 4 Model hardware interfaces with concurrency constructs. (PO3) 5 CO5 Investigate the interface between the test bench and the design of a given system using IEEE1800 Verilog assertions.(PO4)

UNIT - I

Verification Methodologies: The Verification Process, The Verification Plan, The Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, What Should You Randomize, Functional Coverage, Testbench Components, Layered Testbench, Building a Layered Testbench, Simulation Environment Phases, Maximum Code Reuse, Testbench Performance, Conclusion.

UNIT - II

Fundamentals of System Verilog : DATA TYPES, Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width, Net Types, Conclusion, PROCEDURAL STATEMENTS AND ROUTINES, Introduction Procedural Statements,

Tasks, Functions, and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

UNIT - III

Object Oriented Concepts for verification: Think of Nouns, not Verbs, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private, Straying Off Course, Building a Testbench.

UNIT – IV

RANDOMIZATION Techniques for Verification : What to Randomize, Randomization in SystemVerilog, Constraint Details, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post_randomize Functions, Constraints Tips and Techniques, Common Randomization Problems, Iterative and Array Constraints, Atomic Stimulus Generation vs. Scenario Generation, Random Control, Random Generators, Random Device Configuration.

UNIT - V

CONNECTING THE TESTBENCH AND DESIGN: Separating the Testbench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, Connecting It All Together, Top-Level Scope, Program – Module Interactions, SystemVerilog Assertions, The Four-Port ATM Router.

Learning Resources:

1. CHRIS SPEAR Synopsys, Inc. “SYSTEMVERILOG FOR VERIFICATION A Guide to Learning the Testbench Language Features” Springer.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF HUMANITIES AND SOCIAL SCIENCES

Skill Development Course-I: Communication Skills

SYLLABUS FOR M.E. - I SEMESTER

L:T:P (Hrs./week) : 1:0:0	SEE Marks : 40	Course Code: **PI21HS110EH**
Credits : 1	CIE Marks : 30	Duration of SEE : 2 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
This course will enable the students to: 1. involve in the content for all the above mentioned four skills in teaching English and to get students proficient in both receptive and productive skills	On completion of the course the students will be able to: 1. Make effective presentations 2. Successfully attempt versant, AMCAT and secure better placements 3. Perform better in Interviews

UNIT – I : Remedial English: Delightful Descriptions
Describing Past, Present and Future Events.

UNIT - II: Developing Conversational Skills
Exchange of pleasantries, Exchange facts and opinions, Using relevant vocabulary.

UNIT - III: Contextual Conversations:
Ask for Information, Give Information, Convey bad news, show appreciation

UNIT - IV: Business English: **Professional Communication**:
Concise Cogent Communication, Active Listening, Interact, Interpret and Respond. **Expositions and Discussions:** Organization, Key Points, Differing Opinions, Logical conclusions. **Effective Writing Skills:** Structure, Rough Draft, Improvisations and Final Draft for Emails, paragraphs and Essays. **High Impact Presentations:** Structure, Content, Review, Delivery

UNIT - V: Industry Orientation and Interview Preparation
Interview Preparation– Fundamental Principles of Interviewing, Resume Preparation, Types of Interviews, General Preparations for an Interview. Corporate Survival skills: Personal accountability, Goal Setting, Business

Etiquette, Team Work

Learning Resources:

1. Business Communication, by Hory Shankar Mukerjee, Oxford/2013
2. Managing Soft Skills for Personality Development by B.N.Gosh, Tata McGraw-Hill/ 2012
3. Personality Development & Soft Skills by Barun K Mitra, Oxford/2011
4. Murphy, Herta A., Hildebrandt, Herbert W., & Thomas, Jane P., (2008) "Effective Business Communication", Seventh Edition, Tata McGraw Hill, New Delhi
5. Locker, Kitty O., Kaczmarek, Stephen Kyo, (2007), "Business Communication – Building Critical Skills", Tata McGraw Hill, New Delhi
6. Lesikar, Raymond V., &Flatley, Marie E., (2005)"Basic Business Communication – Skills for Empowering the Internet Generation", Tenth Edition, Tata McGraw Hill, New Delhi
7. Raman M., & Singh, P., (2006) "Business Communication", Oxford University Press, New Delhi.

Journals / Magazines:

1. Journal of Business Communication, Sage publications
2. Management Education, Mumbai

Websites:

www.mindtools.com
www.bcr.com

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	20
2.	No. of Assignments	:	2	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	:	2	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF HUMANITIES AND SOCIAL SCIENCES

English for Research Paper Writing

Audit Course - I

SYLLABUS FOR M.E. - I SEMESTER

L:T:P (Hrs./week) : 2:0:0	SEE Marks : 60	Course Code:**PI21AC110EH**
Credits : -	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
This will enable the students should be able to: 1. Understand, how to improve your writing skills and level of readability 2. Learn about what to write in each section 3. Understand the skills needed when writing a Title 4. Ensure the good quality of paper at very first-time submission	On completion of the course, students will be able to 1. write research papers 2. write citations as per the MLA style sheet and APA format 3. write concisely and clearly following the rules of simple grammar, diction and coherence.

UNIT-I:

Planning and Preparation, Word Order, Breaking up long sentences. Structuring Paragraphs and Sentences, Being concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:

Clarifying Who Did What, Highlighting your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT-III:

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, useful phrases, how to ensure paper is as good as it could possibly be the first-time

submission.

UNIT-V:

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

Learning Resources :

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded Systems Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 0:0:3	SEE Marks : -	Course Code:**PI21PC111EC**
Credits : 1.5	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
1. Simulate the replica of hardware environment by implementing desing in Proteus 7.X IDE.	On completion of the course, students will be able to 1. Implement embedded C constructs to configure built-in registers of C51 target. 2. Interface on-chip and off chip peripherals of C51 target. 3. Develop a prototype in proteus software. 4. Compare the architectural features of similar targets for effective design and development. 5. Design and execute a miniproject for the given specifications

List of Experiments using Embedded C/Embedded C++:

1. To toggle LEDs connected to GPIOs of AT89S52 with some intentional Delay.
2. To design & implement 4x3 matrix Keypad Device Driver for ASCII mapping.
3. To design & implement 2x16 LCD Device Driver for displaying below text:

   Line-1: "**Welcome@ESD Lab!**"

   Line-2: "**Enter to Proceed**"
4. To Configure Timer0 and Timer1 for intended delay without interrupts.
5. To design & demonstrate the UART drivers for data transmission and data reception at 9600bps full duplex baud.

6. To design & implement the concept of writing Interrupt Service Routine (ISR) for external interrupt INT0, INT1.
7. To design & implement the concept of mixing of external ISRs with Internal ISRs and understanding the ISR handling process.
8. To design & implement LED Seven Segment driver with adjustable delay.
9. To design & implement User Centric template Menu designs in Embedded C
10. To design and implement embedded C/C++ constructs for programming LPC2148 ARM powered MCU.
11. Mini project based on C51 or LPC2148 target and its execution.

Suggested tools for use:

1. Hardware Target CPU – AT89S52 ; LPC2148 (ARM7 TDMI-S)
2. Embedded Software Development – Keil µVision5 IDE
3. Embedded Debugger – Keil µVision5 Debugger
4. Hardware Simulator – Proteus

The break-up of CIE :

1. No. of Internal Test	:	1
2. Max. Marks for each internal tests	:	12
3. Marks for assessment for day to day evaluation	:	18

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design and Simulation Laboratory - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : -	Course Code:**PI21PC121EC**
Credits : 1.5	CIE Marks : 50	Duration of SEE : -

Course Objectives	Course Outcomes
To demonstrate computer aided design tools for the modeling, design, analysis, test and verification of digital and analog integrated circuits or systems.	On completion of the course, students will be able to 1. Develop HDL code for combinational and sequential logic circuits in various level of abstraction. 2. Synthesize and verify the digital logic circuits on FPGA 3. verify the designs using system Verilog. 4. Simulate the characteristics of inverter under process variations. 5. Design and simulate current mirror and amplifiers.

Part A

1. Design and simulate ALU/Counter using HDL.
2. ASIC Synthesis of ALU/ Counter and find its performance parameters
3. Design a traffic signal controller using finite state machine and implement it on FPGA.
4. Verify test bench of adder using System Verilog.
5. Verify test bench of ALU/ Counter using system Verilog.
6. Insert clock gating for power optimization in ALU/Counter.

PART B

7. Design and Simulation of Symmetrical CMOS inverter and evaluate its performance.
8. Design and simulate a 6-T SRAM cell and find its parameters.
9. Design and simulation of 2 current sources from a reference current source by mirroring and plotting their behaviour.
10. Simulate a single stage MOS amplifier with two different loads and compare their performance.

11. Simulate a differential amplifier with PMOS/ NMOS as input transistors and compare performance.
12. Design and simulate a general purpose CMOS OPAMP.

Note: Minimum of ten experiments are to be conducted.

The break-up of CIE :

1.	No. of Internal Test	:	1
2.	Max. Marks for each internal tests	:	12
3.	Marks for assessment for day to day evaluation	:	18

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Seminar

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : -	Course Code: **PI21PC138EC**
Credits : 1	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. Selection of a suitable topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of seminar report.

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Embedded Systems, VLSI Design and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation

- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION FOR

M.E - ECE (ES&VLSID) EMBEDDED SYSTEMS AND VLSI DESIGN

II-SEMESTER under CBCS Scheme for 2021-22 **(R-21)**

M.E - ECE (ES&VLSID) II-Semester									
S.No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
			Hours per Week			Duration in Hrs	Maximum Marks		Credits
			L	T	P/D		SEE	CIE	
THEORY									
1	PI21PC210EC	PC - IV : Embedded Real Time Operating Systems	3	-	-	3	60	40	3
2	PI21PC220EC	PC - V : Mixed Signal IC Design	3	-	-	3	60	40	3
3	PI21PC230EC	PC - VI : VLSI Physical Design	3	-	-	3	60	40	3
4	PI21PE2X0EC	Professional Elective – III	3	-	-	3	60	40	3
5	PI21OE2XXXX	Open Elective	3	-	-	3	60	40	3
6	PI21HS210EH	Skill Development Course -III: Aptitude	1	-	-	2	40	30	1
7	PI21PE240EC	Skill Development Course -IV: Technical Skills-II	2	-	-	3	60	40	2
8	PI21PC240ME	Research Methodology and IPR	2	-	-	3	60	40	2
9	PI21AC210EH	AC - II : Pedagogy Studies	2	-	-	3	60	40	-
LABORATORY									
10	PI21PC211EC	Embedded System Applications Laboratory	-	-	3	-	-	50	1.5
11	PI21PC221EC	Design and Simulation Laboratory - II	-	-	3	-	-	50	1.5
12	PI21PW219EC	Mini Project	-	-	2	-	-	50	1
		Total	**22**	**-**	**8**		**520**	**500**	**24**
		Grand Total	**30**				**1020**		
Left over hours will be allocated for : Library/ Mentor-Mentee Interaction / FC /CCA									
Note: Every student should acquire one online course certification equivalent to 2 Credits weightage during I to III Semester									

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded Real Time Operating Systems

Professional Core - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC210EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Justify the need of Real Time Operating System for Embedded Product. 2. Discuss RTOS scheduling policies to meet the deadlines along with different inter-process communication resources. 3. Analyze Linux kernel architecture with process & thread related APIs. 4. Categorize device drivers in Linux with corresponding shell commands. 5. Develop system integration with RTOS & acquire debugging techniques.	On completion of the course, students will be able to 1. Differentiate OS, RTOS and classify Real-Time kernels. 2. Demonstrate the use of different scheduling algorithms to estimate the deadline and propose different inter-task-communication models opted in RTOS. 3. Describe Linux kernel architecture and process management. 4. Differentiate Linux user space processes and kernel space threads; and, implement device drivers using Shell APIs. 5. Suggest debugging methods to be opted for RTOS based designs.

UNIT – I

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS; Architecture of RTOS, Kernels – classifications, importance of scheduler in OS: objectives and functions; Hard versus Soft Real-time systems – examples, Jobs & Processes, timing constraints. Pre-emptive Vs Non pre-emptive kernels

UNIT – II

Task Priorities, Scheduling, Inter task Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section: Re-entrant Functions, Inter Process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

Scheduling Algorithms – RMS, Preemptive EDF scheduling – principle, comparisons.

UNIT – III

Linux Kernel 2.x architecture – File system, Concepts of Process – creation, Process Control Block (PCB); process Vs thread; Concurrent Execution. Process Management in Linux – forks Vs Vfork; process state transitions, zombie state, Memory Management Algorithms.

UNIT – IV

Device Drivers – Definition; advantages of Modules; kernel space Vs user space; Concurrency and Race Conditions; classification of device drivers – character drivers, block drivers and net drivers; shell commands for drivers; IOCTLS and Tasklets

UNIT – V

Communicating with Hardware; Interrupt Handling. Debugging Techniques. Comparison of Linux 2.4 Vs 2.6 & 3.x with RT Linux concepts and porting on hardware. Case study of RTOS-RT Linux porting on LPC2148.

Learning Resources:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-to-Use Modules in C", CMP Publishers Jan 1999.
2. Robert Love, "Linux Kernel Development" (3rd Edition), Novell Press 2010.
3. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
4. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, "Linux Device Drivers", 3rd Edition,O'Reilly Media Publishers
5. Real Time Systems, C.M. Krishna and G. Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Mixed Signal IC Design

Professional Core - V

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC220EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Student should clearly distinguish between the features of mixed signal circuits and other circuits. 2. Students would be taught how to arrive at a given mixed signal circuit starting from the specifications 3. Students should be exposed to application areas during the lectures.	On completion of the course, students will be able to 1. This course would generate a class of analog / mixed signal circuit designers 2. They would be able to address problems faced in the realization of systems using mixed signal circuits. 3. Produces a class of students who would be able to analyze a situation in the area of mixed signal circuits like switched capacitor circuits, data converters etc, starting from fundamentals.

UNIT – I

Introduction: concepts involved in mixed signal circuits – Analog & digital operations by the same circuit – Digital and analog circuits on the same substrate – Problems of covering both the types of circuits on the same substrate processes involved in a circuit which has analog / digital signals at the input and digital / analog of the output – mimicking analog components by digital operations (switched capacitor circuits).

Mixed signal functions – comparators sampling and sample and hold operations – Analog to Digital conversion and Digital / Analog conversion – phase and delay locked loops.

UNIT – II

Switched Capacitor Circuits (SCR) – switched capacitor resistor analysis of current and voltage waveforms – S.C.RS in series and parallel – Power dissipation in SCRFET switches charge in injection and clock feed though effects – limitations o f SCRs. Applications of SCR for (i) filters (ii) amplifiers / buffers, Integrators, Voltage multipliers, peak detectors, modulators etc.

Comparators: Basic architecture of a comparator specifications of a comparator op amp based comparator – limitations – modified comparators for improving performance Latched comparators for high speed applications Bi-polar comparators – BiCMOS comparators.

UNIT – III

Sample and hold circuits – specifications MOS sample and hold circuits – clock feed through and charge injection problems – S/H circuits with transmission gates – high input impedance S/H circuit – S/H circuits with improved slewing – Diode bridge based S/H circuits advantages and disadvantages of bridge based S/H circuits. Data converters: Data converter fundamentals performance characteristics – Quantization noise.

UNIT – IV

Data converters, architecture: ideal A/D and D/A converters – Nyquist rate and over sampled D/A converters, philosophy and architectures of Nyquist rate D/A and A/D converters – philosophy and architectures of over sampled converters

Nyquist rate D/A converters: Decoder based converters, binary scaled converters, thermometric code converters, hybrid converters. Nyquist rate A/D converter: Integrating converters, successive approximation converters, Flash or parallel converters two step A/D converter, Cyclic A/D converter, pipe lined A/D converter – VCO based A/D converter.

UNIT – V

Architectures of over sampled A/D converter–1 bit A/D and D/A converters Σ-Δ modulator, noise shaping and noise shaped A/D converter idle tones and dithering–system level description of over sampled A/D and D/A converters

Phase locked loop: What is phase locked loop and its importance in communication and instrumentation electronics–Basic architecture of a PLL-Analog PLL–Digital PLL–Locking limitations–Dynamics of PLL–lock range–Capture range–phase–frequency locked loop-charge pump based PLL–components of PLLs, frequency locked loop–Delay locked loop–applications of PLLs.

Learning Resources:

1. Paul.R. Gray & Robert G. Mayor, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata Mc Grah Hill. 2002.
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Physical Design

Professional Core - VI

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PC230EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To understand the structures of different components of VLSI design. 2. To draw stick and layout diagrams of circuits. 3. To acquire the knowledge of cell based designs.	On completion of the course, students will be able to 1. Design the structures of different components of VLSI design. 2. Apply the basic concepts of physical design to layouts and stick diagrams. 3. Apply Design rules for layouts of circuits. 4. Design hierarchical circuit Layouts using cell concepts. 5. Analyze the basic algorithms which are involved in the process of physical design automation.

UNIT – I

VLSI Design cycles and new trends in Design cycles, physical design cycles and new trends in physical design cycles, Components of VLSI, Various layers of VLSI, Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors ,Brief review of technology , cost and performance analysis.(Reference 1)

UNIT – II

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects), physical design of logic gates – NOT, NAND and NOR. Mask overlays for different structures. Parasitics – latch up and its prevention. Device matching and common centroid techniques for analog circuits(Reference 1 and 3)

UNIT – III

Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams. (Reference 4)

UNIT – IV

Cell concepts – cell based layout design – Wein-berger image array — design hierarchies. System level physical design- large scale physical design , interconnect delay modeling,cross talk, floor planning, routing and clock distribution.(Reference1 and 3)

UNIT – V

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): Basic terminology,graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms. (Referene 1 and 2)

Learning Resources:

1. Algorithms for VLSI Physical Design automation, Naveed Sherwani.3rd edition Kluwer academic publishers
2. Algorithms for VLSI Design automation, Sabith H.Gerez ,John Wiley & sons, Inc.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
4. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
5. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Low Power VLSI Design

Professional Elective - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PI21PE210EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels 2. Apply leakage control mechanisms to reduce static power consumption in DSM VLSI regime 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Study and apply various software power estimation and optimization techniques for low power VLSI system design 5. Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs	On completion of the course, students will be able to 1. Distinguish the impact of various power reduction techniques at different levels of VLSI Design 2. Identify the sources of power dissipation and apply leakage control techniques to reduce static power consumption in CMOS circuits 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Analyze different power reduction techniques for VLSI systems at Design time, Run-time and Stand-by modes 5. Employ software power estimation and optimization methods for low power VLSI system design 6. Apply low power circuit and architectural techniques such as capacitance reduction, gated clocking, VDD and Vth scaling, DVS etc in digital systems and SRAM designs

UNIT – I

Introduction to Low Power design: Why worry about power – at global and SOC levels, Emerging zero-power applications (WSN), 20 nm scenario, Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels)

Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design – Standby leakage control using transistor stacks, Multiple V_{TH} and dynamic V_{TH} techniques, Supply voltage scaling technique (Ref-1)

UNIT – II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent

Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories (Ref-2)

UNIT – III

Power Optimization Techniques – II: Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues (Ref-2) Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power (Ref-3)

UNIT - IV

Low Voltage Low Power Static Random Access memories**:** Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, Loadless CMOS 4T SRAM cell, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction (Ref-1)

UNIT - V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, Varying the clock speed, varying the V_{DD} of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

Learning Resources:

1. Kiat-Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata McGrawhill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, " Low-Power CMOS VLSI Circuit Design" , Wiley Pub., 2000 (Unit III)
4. Dimitrios Soudris, Christian Piguet and Coastas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002 (Topics beyond Syllabus)
5. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010 (for seminars and assignments)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Hardware-Software Co-design

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE220EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To understand architectures, co-design methodology and design	On completion of the course, students will be able to 1. Identify the need for co-design 2. Model data flow and implement the same through software and hardware 3. Construct data flow and control flow graphs 4. Design data flow model for a FSM 5. Design an SoC for given application

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs,

compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level
specification languages, Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Learning Resources:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CPLD & FPGA Architectures and Applications

Professional Elective - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE230EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Implement given task using FPGA 2. Develop test pattern to test the FPGA 3. Design a product level approach utilizing FPGAs.	On completion of the course, students will be able to 1. Differentiate between ROM, PAL, PLA, SPLD, CPLD, FPGA. 2. Compare the features of Various CPLDs interms of their architecture, Logic blocks. 3. Compare the features of Various FPGAs interms of their Architecture, Configurable logic block and routing. 4. Gain knowledge on routing algorithms adopted in FPGAs. 5. Test a particular PLD using various techniques like design validation, Timing verification.

UNIT – I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT – II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's-XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT – III

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT – IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT – V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps.
Verification: introduction, logic simulation, design validation, timing verification.
Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Learning Resources:

1. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Pearson Education 2009.
2. S. Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S. Brown, R. Francis, J. Rose, Z.Vransic, Field Programmable Gate array, Kluwer Publn, 1992.
5. Manuals from Xilinx, Altera, AMD, Actel.

The break-up of CIE : Internal Tests + Assignments + Quizzes

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Fundamentals of Python Programming

Open Elective

SYLLABUS FOR M.E. II-SEMESTER

L:T:P(Hrs./week): 2:0:0	SEE Marks : 60	Course Code: **PX21OE210CS**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES		**COURSE OUTCOMES** On completion of the course, students will be able to	
1	Acquire problem solving skills	1	Develop Python programs with conditional statements and loops.
2	Write programs using Python language	2	Write programs using functions,
		3	Construct Python data structures programs using Strings Lists
		4	Design programs using tuples, and set.
		5	Develop programs using dictionaries

UNIT-I:

Basics of Python Programming: Features of Python**,** variables and identifiers, operators and expressions.

Decision control Statements: Selection/Conditional branching statements,

basic loop structures/iterative Statements, nested loops, break, continue, and pass Statements.

UNIT-II:

Functions and Modules: function definition, function call, more on defining functions, recursive functions, modules.

UNIT –III:

Data Structures: Strings :Introduction, built-in string methods and functions, slice operation, String Module. Regular Expressions.

Lists : Introduction, nested list, cloning lists, basic list operations, list methods. Functional programming-filter(),map(),reduce() function.

UNIT-IV:

Tuples : Introduction, basic tuple operations, tuple assignment, tuples for returning multiple values, nested tuples, tuple methods and functions.

Set: Introduction, Set operations.

UNIT-V:

Dictionaries : Basic operations, sorting items, looping over dictionary, nested dictionaries, built-in dictionary functions.

Learning Resources:

1. Reema Thareja ,"Python programming using problem solving approach ", Oxford university press.
2. Allen Downey," Think Python: How to Think Like a Computer Scientist", O'Reilly publications,2nd Edition.
3. Albert Lukaszewski, "Mysql for python ", PACKT publishers
4. Mark Lutz , "Learning Python",O'Reilly Publications.
5. Stewart Venit and Elizabeth Drake, Prelude to Programming: Concepts and Design, 6th Edition(2015), Pearson India
6. Mark J Guzdial, Introduction to Computing and programming in Python, 3rdEdition(2013), Pearson India
7. http://nptel.ac.in/courses/117106113/34
8. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-01sc-introduction-to-electrical-engineering-and-computer-science-i-spring-2011/python-tutorial/
9. www.scipy-lectures.org/intro/language/python_language.html

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Industrial Safety

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE220XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT – I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment. Model Curriculum of Engineering & Technology PG Courses [Volume -II] 295

UNIT - III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,

v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Learning Resources:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF MECHANICAL ENGINEERING

Advanced Operations Research

Open Elective

SYLLABUS FOR M.E. II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE230ME**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The objective of this course is to: understand Linear & non-linear programming, transportation modelling , CPM & PERT for project scheduling and control, replacement, game theory and sequencing	On completion of the course, the student will be able to: 1. understand simplex, dual simplex, Sensitivity and transportation and their applications for shop floor problems. 2. understand the importance of Sensitivity analysis and various advanced LPP techniques 3. apply the techniques like CPM and PERT for project management. 4. apply various replacement techniques to find optimum replacement time period for equipment. 5. identify the best strategy to win the game and optimum sequence for minimum elapsed time.

UNIT-I: OPERATIONS RESEARCH-AN OVERVIEW

Meaning and Origin of Operations research, Introduction to Linear programming problems (LPP) -Formulation of LPP-Solution to LPP by Graphical method and simplex method.

UNIT-II: ADVANCED TOPICS IN LINEAR PROGRAMMING

Dual simplex method, special cases in LPP, Duality in LPP, Differences between primal and dual, shadow prices, sensitivity analysis. Non linear programming Khun Tucker conditions.

UNIT-III

Transportation Model: Definition of the transportation model-matrix of Transportation model-Formulation and solution of transportation models-Methods for calculating Initial basic feasible solution, optimal solution by Stepping stone method and MODI method.

Assignment Problem: Hungarian method of assignment problem, maximization in assignment problem, unbalanced problem, problems with restrictions, travelling salesman problems.

UNIT-IV: PROJECT SCHEDULING

Introduction to network analysis, Rules to draw network diagram, Fulkerson rule for numbering events, Critical path method, Summarisation of CPM calculations. PERT, Estimation of probability and its corresponding duration in PERT, Crashing of project and finding of optimal project duration in crashing.

UNIT-V

Replacement models: Introduction, replacement of items that deteriorate ignoring change in money value, replacement of items that deteriorate considering change in money value with time, replacement of items that fail suddenly – individual replacement policy, group replacement policy.

Game theory: Introduction, 2 person zero sum games, maximi– minima principle, principle of dominance, solution for mixed strategy problems graphical method for 2 x n and m x 2 games

Sequencing models: introduction, general assumptions, processing to jobs through 2 machines, processing 'n' jobs through m machines processing 2 jobs through m machines.

Learning Resources:

1. S. D.Sharma, "Operations Research", 10th edition, Newage India Pvt Ltd, New Delhi
2. Hamady.A.Taha An Introduction to Operations Research, "8th edition, TMH
3. Prem Kumar Gupta and Dr. DS Hira, "Operations Research ", S.Chand & Company Pvt. Ltd., 2014.
4. R. Paneerselvam, "Operations Research", PHI Learning Pvt Ltd., 2009.
5. NVS Raju, "Optimization methods for Engineers ", PHI Learning Pvt. Ltd. ., 2014
6. Col D.S. Cheema, "Operations Research", University science press, 2nd edition, India

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Cost Management of Engineering Projects

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE340XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

Introduction and Overview of the Strategic Cost Management Process Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Learning Resources:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Composite Materials

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE250XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT–I

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount

truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Learning Resources:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.
3. Hand Book of Composite Materials-ed-Lubin.
4. Composite Materials – K.K.Chawla.
5. Composite Materials Science and Applications – Deborah D.L. Chung.
6. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Waste to Energy

Open Elective

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE360XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT-I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT – III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for Model Curriculum of Engineering & Technology PG Courses [Volume -II] 299 thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT - IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT – V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants –

Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Learning Resources:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

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3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEAPRTMENT OF HUMANITIES AND SOCIAL SCIENCES

Business Analytics

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PX21OE270XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Understand the role of business analytics within an organization. 2. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization. 3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making. 4. To become familiar with processes needed to develop, report, and analyze business data. 5. Use decision-making tools/Operations research techniques. 6. Mange business process using analytical and management tools. 7. Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.	On completion of the course, students will be able to 1. Students will demonstrate knowledge of data analytics. 2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics. 3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making. 4. Students will demonstrate the ability to translate data into clear, actionable insights

UNIT -I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT - II

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business

Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT – III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization

UNIT – IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT – V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

UNIT – VI

Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Learning Resources:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

The break-up of CIE : Internal Tests + Assignments + Quizzes

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DEPARTMENT OF MECHANICAL ENGINEERING

Research Methodology and IPR

SYLLABUS FOR M.E. - II SEMESTER

L:T:P (Hrs./week) : 2:0:0	SEE Marks : 60	Course Code:**PI21PC240ME**
Credits : 2	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The objectives of this course are to: 1. Learn the research methodology and formulation. 2. Know the sources of literature, method for collection of research data and report writing. 3. Understand IPR laws and Acts.	On completion of the course, students will be able to 1. Explain objectives of research and research process. 2. search the relevant literature and summarize information for formulating the research problem. 3. collect and organize the data for the preparation of research report. 4. explain different types of intellectual property rights and related laws. 5. understand the patent administration system.

UNIT - I

Research Methodology: Meaning of research, Objectives and motivation of research, types of research, research approaches, significance of research, research methods versus methodology, criteria of good research, Research problem formulation.

UNIT - II

Literature survey: Importance of literature survey, sources of information, Literature review: Need of Literature review, Plagiarism, research ethics, errors in research, Assessment of quality of journals.

UNIT - III

Data collection & report preparation: Collection of primary data, secondary data, data organization, methods of data grouping, diagrammatic representation of data, graphic representation of data. Effective technical writing and how to write report, format of a research proposal, contents of a standard technical journal/conference paper, contents of dissertation.

UNIT - IV

Introduction to Intellectual property law: Basics and types of intellectual property, international organizations, agencies and treaties.

Law of Trademarks: Purpose and functions of trademarks, types of Marks, acquisition of trade mark rights, protectable matter and trade mark registration process, Trade Mark Act.

UNIT - V

Law of copyrights: Introduction, common law rights. Rights of reproduction, rights to display work publicly, other limitations of exclusive rights, copyright ownership issues, copy right registration and Berne convention.

Law of Patents: Administration of Indian patent system, Introduction, rights under patent law. Design patents, Plant patents. Patenting process. Patent ownership and transfer, new developments in IPR and international patent laws, Geographical Indications.

Learning References:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'.
2. C. R. Kothari-Research Methodology Methods and Techniques, Second revised edition, New Age International (P) limited Publishers, New Delhi.2013.
3. Ranjitkumar, Research methodology, A step-by-step Guide for Beginners, second Edition, Sage Publications India Pvt. Ltd, New Delhi.2017.
4. Panneer Selvam, Research Methodology, Second Edition, PHI Learning Pvt. Ltd, New Delhi.
5. Deborah E. Bouchoux -Intellectual Property, the law of trademarks, Copyrights, Patents and Trade Secrets. Fourth Edition, CENGAGE Learning India private Limited, New Delhi.2013.
6. P. Narayana, Intellectual property law, Third Edition, Eastern Law House, New Delhi.

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DEAPRTMENT OF HUMANITIES AND SOCIAL SCIENCES

Pedagogy Studies

Audit Course - II

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 2:0:0	SEE Marks : 60	Course Code: **PI21AC210EH**
Credits : -	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
This course will enable the students to: 1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. 2. Identify critical evidence gaps to guide the development.	On completion of the course, students will be able to 1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries? 2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners? 3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit	Content
1a.	**Introduction and Methodology :** ➢ Theories of learning, Curriculum, Teacher education. ➢ Conceptual framework, Research questions. ➢ Overview of methodology and Searching. ➢ Pedagogic theory and pedagogical approaches. ➢ Teachers' attitudes and beliefs and Pedagogic strategies.
b.	**Thematic overview:** ➢ Pedagogical practices that are being used by teachers. ➢ Curriculum, Teacher education. How can teacher education (curriculum and practicum) and the curriculum and guidance materials best support effective pedagogy.

2	• **Research gaps and future directions** ➢ Research design- Lesson plans, Course plans ➢ Teacher education ➢ Curriculum and assessment

Learning Resources:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

The break-up of CIE : Internal Tests + Assignments + Quizzes

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2.	No. of Assignments	:	3	Max. Marks for each Assignment	:	5
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded System Applications Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 0:0:3	SEE Marks : -	Course Code: **PI21PC211EC**
Credits : 1.5	CIE Marks : 50	Duration of SEE : 3 Hours

Course Objectives	Course Outcomes
1. Acquire skills to handle ARM powered cross compilers and Validate different RTOS scheduling algorithms in embOS RTOS and linux.	On completion of the course, students will be able to 1. Demonstrate host to ARM target communication in embOS RTOS environment. 2. Configure emPower board with embOS and validate different scheduling algorithms. 3. Demonstrate different IPC schemes for multi-tasking in embOS and Linux OS. 4. Debug embedded application in RTOS with Cortex M4F ARM target and Linux OS. 5. Customize RTOS application with ARM MCU/Linux OS

List of Experiments in RTOS using Embedded – C/C++:

S.No	Experiment
1.	ADC0804/ADC0808 Interfacing.
2.	SAR DAC 0808 Interfacing.
3.	Linux/emboss Real time task creation, Demonstration of Multitasking
4.	Round Robin Architecture in RTOS
5.	Round Robin with Preemption
6.	Multitasking

7. IPC Techniques in RTOS- semaphores
8. IPC Techniques in RTOS- Pipes
9. IPC Techniques in RTOS- Mutex
10. Shared memory Access
11. Client server Process
12. System calls
13. Thread Process
14. Child – Parent Process

Suggested tools for use:

1. Hardware Target CPU - Cortex M4F powere Segger Board,AT89S52
2. Embedded Software Development - Embedded Studio V3.12a
3. Embedded Debugger - Cortex M4F ARM Jlink
4. RTOS - Linux/emboss

The break-up of CIE :

1.	No. of Internal Test	:	1
2.	Max. Marks for each internal tests	:	12
3.	Marks for assessment for day to day evaluation	:	18

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design and Simulation Laboratory - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 0:0:3	SEE Marks : -	Course Code: **PI21PC221EC**
Credits : 1.5	CIE Marks : 50	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To Design and simulate basic building blocks of mixed signal IC's and perform full custom design of cells .	On completion of the course, students will be able to 1. Perform floor planning, placement and routing of ALU/Counter. 2. Perform layout and paracitic extraction of ALU/Counter. 3. Design and simulate ADC and DAC converters. 4. Design and simulate the basic building blocks of analog and mixed signal integrated circuits. 5. perform full custom design of cells of integrated circuits.

Part A

1. Floor planning, placement and routing of ALU/ Counter.
2. Layout and parasitic extraction of ALU/ Counter.
3. Static timing analysis and power analysis of of ALU/ Counter.
4. Layout of basic gates. (inverter/Nand/NOR, Full custom design).
5. DRC and LVS of basic gates. (inverter/Nand/NOR, Full custom design).
6. Parasitic extraction and Post layout simulation of basic gates. (inverter/Nand/NOR, Full custom design).
7. Insert the scan chains into the design to improve the testability.

Part -B

8. Design and simulation of VCO.
9. Design and simulate the current starved Voltage controlled Oscillator and compare its performance with VCO.
10. Design and simulate latched based comparator.
11. Design and simulate 4-bit current steering DAC.
12. Design and simulate 3/4 bit Flash ADC.

Note: Minimum of ten experiments are to be conducted.

The break-up of CIE :

1.	No. of Internal Test	:	1
2.	Max. Marks for each internal tests	:	12
3.	Marks for assessment for day to day evaluation	:	18

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Mini Project

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 0:0:2	SEE Marks : -	Course Code: **PI21PW219EC**
Credits : 1	CIE Marks : 50	Duration of SEE : 3 Hours

Course Objectives	Course Outcomes
Understand the real world problems and find the required solution.	On completion of the course, students will be able to 1 Understand of contemporary / emerging technology for various processes and systems. 2 Create solutions to the real world problems. 3 Share knowledge effectively in oral and written form and formulate documents.

The introduction of mini projects ensures preparedness of students to undertake major projects/dissertation.

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION FOR

M.E - ECE (ES&VLSID) : EMBEDDED SYSTEMS AND VLSI DESIGN

III - SEMESTER under CBCS Scheme for 2022-23 **Batch (R-21)**

M.E - ECE (ES&VLSID) III- Semester									
S.No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
			Hours per Week			Duration in Hrs	Maximum Marks		Credits
			L	T	P/D		SEE	CIE	
1	PI21PE3X0EC	Professional Elective – IV	3	-	-	3	60	40	3
2	PI21PE3X0EC	Professional Elective – V	3	-	-	3	60	40	3
3	PI21PW319EC	Dissertation-Phase-I / Internship	-	-	8	-	-	100	4
		TOTAL	**6**	**-**	**8**		**120**	**180**	**10**
		GRAND TOTAL	**14**				**300**		

Note: Every student should acquire one online course certification equivalent to 2 Credits weightage during I to III Semester

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Physical Design Automation

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE310EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will develop placement and routing algorithms for VLSI Designs using C / C++.	On completion of the course, students will be able to 1. understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology. 2. adapt the design algorithms to meet the critical design parameters. 3. map various layout optimization techniques to the algorithms. 4. develop proto-type EDA tool and test its efficacy.

UNIT-I : VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost. Factors,

UNIT-II: Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and
Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

UNIT-III: Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

UNIT-IV: Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT-V: Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Learning Resources:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

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3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

High Level Synthesis

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PI21PE320EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

Course Objectives	Course Outcomes
To expose the students, the basics of FPGA designs and synthesis.	On completion of the course, students will be able to 1 Develop simple arithmetic modules and implement in FPGA .(PO1, PO5) 2 Understand various libraries used in HLS based design (PO2) 3 Apply various coding styles for FPGA synthesis and compare their performance (PO1, PO2) 4 Compare the precision data types in System C and Vivado HLS (PO2, PO3) 5 Synthesize a subsystem design using Vivado HLS and port it in FPGA (PO3, PO5)

UNIT – I

Introduction to C-based FPGA Design, Using Vivado HLS HLS UltraFast Design Methodology Managing Interfaces Design Optimization RTL Verification, Exporting the RTL Design

UNIT – II

Introduction to the Vivado HLS C Libraries, Arbitrary Precision Data Types Library, The HLS Stream Library, HLS Math Library, Vivado HLS Video Library, The HLS IP Libraries, HLS Linear Algebra Library.

UNIT – III

Coding Styles: Unsupported C Constructs, The C Test Bench Functions, Loops, Arrays, Data Types. C++ Classes and Templates, Using Assertions, SystemC Synthesis.

UNIT – IV

Command Reference, Graphical User Interface (GUI) Reference, Send Feedback, Interface Synthesis Reference, AXI4 Slave Lite C Driver Reference, Video Functions Reference.

UNIT – V

HLS Linear Algebra Library, C Arbitrary Precision Types, C++ Arbitrary Precision Types, C++ Arbitrary Precision Fixed Point Types, Comparison of SystemC and Vivado HLS Types.

Learning Resources:

1. Andres Takach, Creating C++ IP for High Performance Hardware Implementations of FFTs. DesignsDesignCon2002.
2. Preston A. Jackson, Cy P. Chan, Jonathan E. Scalera, Charles M. Rader, and M. Michael Vai - A Systolic FFT Architecture for Real Time FPGA Systems. MIT Lincoln Laboratory 244 Wood ST, Lexington, MA 02420
3. Vivado Design Suite User Guide and Vivado Design Suite Tutorial for High-Level Synthesis.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

System on Chip (SoC) Design

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE330EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
This course covers the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of system design. The course enables students to apply their knowledge for the design of advanced digital hardware systems with help of FPGA tools. 1. Understand the FPGA hardware architecture and interconnect technologies. 2. Apply the knowledge for the design of digital hardware systems. 3. Implementation of FPGA implementation methodologies with the help of FPGA tools. 4. Block level design verification by writing the test benches. 5. System level design verification by writing the test cases.	On completion of the course, students will be able to 1. Understand design flow of SoC 2. Implement the basic level logic functions in hardware system. 3. Implement the block level and system level IP cores. 4. Writing test benches for block level design verification. 5. Writing test benches for system level design verification.

UNIT - I

Introduction to SoC Design, constituents of SoC, Application areas of SoC, SoC development life cycle FPGA architectures for implementing SoC design, FPGA based SoC design flow.

UNIT - II

Front End Design and Back-End Design Overview, Programmable system on chip design, Design with Xilinx zynq SoC platform, Implementation examples of logic functions using LUTs and CLBs, Finite state machine design examples.

UNIT - III

Introduction to IP cores, Block level design using IP cores, Implementation of Block RAM using IP cores, FIFO design and implementation using IP cores.

UNIT - IV

Block Level Design Verification: Introduction to Block-level verification, verification approaches, Functional verification, Static timing verification, Front End Design stages in detail-Flow: Architecture, Design Entry, Simulation, Synthesis and Verification, 16 bit ALU design verification with VIO hardware debugger, Constraints and timings analysis.

UNIT - V

System Level Design Verification: Introduction to system level verification, creating system-level test benches, Applying and migrating test bench-SoC, Design challenges and approaches.

Learning Resources:

1. Veena S. Chakravarthi, "A practical Approach to VLSI System on Chip (SoC) Design", A comprehensive Guide, Springer.
2. Prakash Rashinkar, Peter Paterson and Leena Singh "System-on-a-Chip Verification – Methodology and Techniques", Kluwer Academic Publishers.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design for Testability

Professional Elective - V

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **PI21PE340EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To expose the students, the basics of testing techniques for circuits.	On completion of the course, students will be able to 1. Illustrate Yield, Fabrication defects, Errors and Faults in VLSI Circuits 2. Simulate digital ICs in the presence of faults and evaluate the given test set for fault coverage. 3. Generate test patterns for detecting single stuck faults in combinational and sequential circuits. 4. Establish a fault model for memory and apply March Tests for fault detection 5. Identify schemes for introducing testability into digital circuits with improved fault coverage. 6. Compare different approaches for introducing BIST into logic circuits, memories and embedded cores.

UNIT – I

Introduction: Role of Testing, Digital and Analog VLSI Testing, The Rule of TEN, Yield, Defects and Faults, Reliability and Failure Rate, Test and Design for Testability (DFT)

Modeling: Modeling digital circuits at logic level, register level and structural models.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event- driven simulation. {Ref1: Chs 1,2,3 and Ref2: Ch3)

UNIT – II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence, Fault location and Fault Collapsing, The Single Stuck and Multiple Stuck Fault Models. Bridging Faults, CMOS Technology Considerations, Intermittent Faults

Fault Simulation: Applications, Fault Simulation for Combinational circuits. (Ref1: Chs 4 and 5)

UNIT – III

Testing for single stuck faults (SSF): Automated Test Pattern Generation (ATPG/ATG) for SSFs in Combinational Circuits, Algorithms (D, PODEM, FAN), ATG for SSFs in Sequential Circuits. Functional Testing without and with Specific Fault Models

Memory Test: Memory density and Defect trends, Faults, Memory Test levels, March Test Notation, Fault Modeling, Memory Testing {Ref1: Chs 6 and 8, Ref2: Ch 9)

UNIT – IV

Design for Testability – Controllability and Observability, AdHoc DFT techniques. Scan architectures and testing – Generic boundary scan, Full Serial integrated scan, Storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – Syndrome test and Signature analysis – LFSR based Signature Analysis (Ref1: Chs 9 and 10)

UNIT – V

Built-in Self-Test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures in brief.

System Test and Core-Based Design: System Test Problem Defined, Functional Test, Diagnostic Test, Testable System design, Core-Based Design and Test –Wrapper, A Test Architecture for SOC, An Integrated Design and Test Approach. {Ref1: Ch 11, Ref2: Ch 18}

DSP-based Analog and Mixed-Signal Test: Functional DSP-based Testing, Static ADC/DAC Testing Methods, CODEC Testing, Dynamic Flash ADC Testing using FFT Technique. {Ref2: Ch 10).

Learning Resources:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
2. Michael L Bushnell and Vishwani D Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits" Kluwer Academic Publishers, 2002
3. NPTEL Course on VLSI Testing – IIT Kharagpur

The break-up of CIE : Internal Tests + Assignments + Quizzes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Scripting Languages

Professional Elective - V

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE350EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To understand control structures of perl. 2. To classify character classes. 3. To apply subroutines and data structures. 4. To acquire the knowledge extending perl. 5. To understand broad features of SKILL, CGI.	On completion of the course, students will be able to 1. Design control structures of perl. 2. Apply subroutines and data structures. 3. Extend perl to embedding perl. 4. Classify character classes. 5. Model features of SKILL, CGI.

UNIT – I

Overview of scripting languages-PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT – II

Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT – III

Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions. Inter process communication,- signals, files, pipes, sockets,.

UNIT – IV

Threads- process model, thread model, Perl debugger- using debugger commands, customization, internals and externals, internal data types, extending Perl, embedding Perl, exercises for programming using Perl.

UNIT – V

Other languages: Broad features of other scripting languages SKILL, CGI, java script, VB script.

Learning Resources:

1. Larry Wall, Tom Christiansen, John Orwant, "programming perl", oreilly publications, 3rd edition.
2. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly publications.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Static Timing Analysis

Professional Elective - V

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **PI21PE360EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will 1 understand clock domains and critical paths in a given logic design 2 Interpret extracted parasitics and reduce parasitics in critical paths 3 Estimate the Interconnect delays and calculate multiple path slacks 4 Perform cross-talk and Noise analysis in a given net 5 Perform timing analysis and verification across multicycle paths and clock domains	On completion of the course, students will be able to 1. Identify critical paths and estimate propagation delays and skews in a given data-path (PO1 and PO2) 2. Compare the performance of Elmore delay model and higher order interconnect delay models (PO3) 3. Analyse Cross-talk Noise and its reduction in a given data path (PO2) 4. Perform timing analysis across multicycle paths and interpret the results (PO2, PO5) 5. Estimate the timing across multiple clock domains and refine the timing by path balancing (PO2, PO3 and PO5)

UNIT – I

STA Concepts : CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions.

UNIT – II

Interconnect Parasitics: RLC for Interconnect, T-model, Pi-model, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets.

UNIT – III

Delay Calculations: Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging , Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation , Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths Slack Calculation.

UNIT – IV

Crosstalk and Noise Analysis: Crosstalk Glitch Analysis, Basics Types of Glitches, Rise and Fall Glitches, Overshoot and Undershoot Glitches, Glitch Thresholds and Propagation, DC Thresholds, AC Thresholds, Noise Accumulation with Multiple Aggressors, Aggressor Timing Correlation, Aggressor Functional Correlation, Crosstalk Delay Analysis, Basics, Positive and Negative Crosstalk, Accumulation with Multiple Aggressors, Aggressor Victim Timing Correlation, Aggressor Victim Functional Correlation, Timing Verification Using Crosstalk Delay, Setup Analysis, Hold Analysis, Computational Complexity, Hierarchical Design and Analysis, Filtering of Coupling Capacitances, Noise Avoidance Techniques.

UNIT – V

STA Environment & Timing Verification : What is the STA Environment, timing issues, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Constraining Output Paths, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Multicycle Paths, Crossing Clock Domains, False Paths, Half-Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Examples, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks.

Learning Resources:

6. J. Bhasker, Rakesh Chadha “Static Timing Analysis for Nanometer Designs A Practical Approach” springer, 2009.

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Dissertation - Phase - I / Internship

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 0:0:8	SEE Marks: -	Course Code: **PI21PW319EC**
Credits : 4	CIE Marks: 100	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
1. Selection of a suitable for investigation for the project 2. Literature survey 3. Carrying out investigation / experiments including the selection of approaches to be adopted 4. Analysis of the results in interaction with the project guides. 5. Preparation of presentations and technical report.	On completion of the course, students will be able to 1. Students go through the foundation needed for carrying out new investigations 2. Students would be ready with the problem to be investigated in phase II 3. They also get the training needed for presentations of their work.

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.
All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.
The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

+ Excellent /Very Good / Good/Satisfactory / Unsatisfactory

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
DEPARTMENTOF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHEME OF INSTRUCTION AND EXAMINATION FOR

M.E - ECE (ES&VLSID) : EMBEDDED SYSTEMS AND VLSI DESIGN

IV-SEMESTER under CBCS Scheme for 2022-23 Batch (R-21)

M.E - ECE (ES&VLSID) IV-SEMESTER									
S. No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
			Hours per Week			Duration in Hrs	Maximum Marks		Credits
			L	T	P/D		SEE	CIE	
1	PI21PW419EC	Dissertation-Phase-II / Internship	-	-	20	-	Viva-Voce (Grade)		**10**
		MOOCs Certification Course : 8 or 12 weeks duration	-	-	-	-	-		**2**
TOTAL			**-**	**-**	**20**	**-**	**-**	**-**	**12**
GRAND TOTAL			**20**						

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Dissertation - Phase - II / Internship

SYLLABUS FOR M.E. ECE (ES&VLSID) - IV SEMESTER

L:T:P(Hrs./week):0:0:20	SEE Marks: -	Course Code: **PI21PW419EC**
Credits : 10	CIE Marks: **Viva-Voce Grade**	Duration of SEE:

COURSE OBJECTIVES	COURSE OUTCOMES
1. Carrying out further literature survey related to the topic already selected. 2. Carrying out investigation experiments, simulation in relation to the problem. 3. Problem analysis and solution finding for problems encountered 4. Organization of results 5. Thesis preparation, presentation and defence.	On completion of the course, students will be able to 1. Students will be able to face any new problem and find a sensible solution 2. Students would be trained to investigate a given problem in a systematic way 3. They would be ready to take up work which may be needed by the industry.

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

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