# VASAVI COLLEGE OF ENGINEERING
# (AUTONOMOUS)

ACCREDITED BY NAAC WITH 'A++' GRADE

Ibrahimbagh, Hyderabad-31

Approved by A.I.C.T.E., New Delhi and

Affiliated to Osmania University, Hyderabad-07

**Sponsored**

**by**

**VASAVI ACADEMY OF EDUCATION**

**Hyderabad**

## SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR

## Bachelor of Engineering (ECE)

**with**

## Honours Degree in System on Chip Design

**With effect from 2022-23**

**(For the batch admitted in 2020-21)**

**(R-20)**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Phones: +91-40-23146040, 23146041

Fax: +91-40-23146090

## Institute Vision

Striving for a symbiosis of technological excellence and human values

## Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

## Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering and fostering ethical values

## Department Mission

To inculcate a spirit of scientific temper and analytical thinking and train the students in contemporary technologies in Electronics and Communication Engineering to meet the needs of the industry and society with ethical values

| B.E (ECE) Program Educational Objectives (PEO's) | |
|---|---|
| **PEO I** | Graduates will be able to identify, analyze and solve engineering problems. |
| **PEO II** | Graduates will be able to succeed in their careers, higher education, and research. |
| **PEO III** | Graduates will be able to excel individually and in multidisciplinary teams to solve industry and societal problems. |
| **PEO IV** | Graduates will be able to exhibit leadership qualities and lifelong learning skills with ethical values. |

| B.E. (ECE) PROGRAM OUTCOMES (PO's)<br>Engineering Graduates will be able to: | |
|---|---|
| **PO1** | Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems. |
| **PO2** | Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences. |
| **PO3** | Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal and environmental considerations. |
| **PO4** | Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions. |
| **PO5** | Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations. |
| **PO6** | The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice. |
| **PO7** | Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development. |
| **PO8** | Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. |
| **PO9** | Individual and team work: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings. |
| **PO10** | Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions. |
| **PO11** | Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. |
| **PO12** | Lifelong learning: Recognize the need, and for have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change. |

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION **(R-20)**

# Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

| B.E (ECE) Hononrs Degree in SoC Design | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S. No. | Course Code | Name of the Course | Scheme of Instruction | | | Scheme of Examination | | | Credits | Semester |
| | | | Hours per Week | | | Duration in Hrs | Maximum Marks | | | |
| | | | L | T | P | | SEE | CIE | | |
| 1. | U20PC550EC | Advanced System Design | 2 | - | - | 3 | 60 | 40 | 2 | V |
| 2. | U20PC551EC | Advanced System Design Lab | - | - | 2 | 3 | 50 | 30 | 1 | V |
| 3. | U20PC650EC | Field Programmable Gate Array (FPGA) Based System Design | 2 | - | - | 3 | 60 | 40 | 2 | VI |
| 4. | U20PC651EC | Field Programmable Gate Array (FPGA) Based System Design Lab | - | - | 2 | 3 | 50 | 30 | 1 | VI |
| 5. | U20PC730EC | Design Verification | 2 | - | - | 3 | 60 | 40 | 2 | VII |
| 6. | U20PC731EC | Design Verification Lab | - | - | 2 | 3 | 50 | 30 | 1 | VII |
| 7. | U20PW729EC | Course Project | - | - | 6 | 3 | 60 | 40 | 3 | VII |
| | | **Total** | **6** | **-** | **12** | | **390** | **250** | **12** | |
| | | **Grand Total** | **18** | | | | **640** | | | |
| 8. | NPTEL Courses : SoC related 2 NPTEL courses with 12 weeks duration | | | | | | | | **6** | V to VII |
| | | | | | | | | **Total Credits** | **18** | |
| Note: Students willing to Opt B.E (ECE) Honours Degree in System on Chip Design shall complete one NPTEL Course Certification (equivalent to 2 Credits weightage) by the end of IV-Semester. | | | | | | | | | | |

## NPTEL Courses Recommended by the ECE Department (R-20)

| S.No. | Title | Instructor | Name of the College | Duration |
|---|---|---|---|---|
| 1. | VLSI Physical Design | Prof. Indranil Sengupta | IIT Kharagpur | 12 weeks |
| 2. | VLSI Design Verification and Test | Dr. Santosh Biswas<br>Prof. Jatindra Kumar Deka | IIT Guwahati | 12 weeks |
| 3. | Analog IC Design | Dr. Nagendra Krishnapura | IIT Madras | 12 weeks |
| 4. | CMOS Analog VLSI Design | Prof. A.N. Chandorkar | IIT Bombay | 12 weeks |
| 5. | Digital VLSI Testing | Prof. Santanu Chattopadhyay | IIT Kharagpur | 12 weeks |
| 6. | Embedded System Design with ARM | Prof. Indranil Sengupta<br>Prof. Kamalika Dutta | IIT Kharagpur | 12 weeks |

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Advanced System Design

SYLLABUS FOR B.E. V – SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs/Week): 2:0:0 | SEE Marks: 60 | Course Code: **U20PC550EC** |
| Credits: 2 | CIE Marks: 40 | Duration of SEE: 3 Hours |

| COURSE OBJECTIVES | COURSE OUTCOMES |
|---|---|
| 1. Justify the philosophy of ARM core as CPU in SoC designs.<br>2. Demonstrate ARM ISA Assembly usage for data processing.<br>3. Implement and Debug embedded drivers in C for Cortex M4 MCU. | On completion of the course, students will be able to<br>1. Summarize ARM based SoC design principles for efficient system design.<br>2. Describe Cortex M4 Core Architecture and Interrupt processing.<br>3. Construct programs using ARM ISA Assembly for data processing needs.<br>4. Design & Validate embedded C drivers for on-chip peripherals of STM32.<br>5. Realize a complete system using ARM Cortex M4 with different I/Os. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 2 | 2 | 2 | 1 | 2 | | | | | | | 1 | 2 | 2 | 1 |
| CO2 | 2 | 2 | 2 | 1 | 2 | | | | | | | 1 | 2 | 2 | 1 |
| CO3 | 3 | 2 | 3 | 2 | 3 | | | | 1 | | | 1 | 2 | 2 | 1 |
| CO4 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | | 1 | 2 | 2 | 1 |
| CO5 | 1 | 2 | 3 | 1 | 2 | | | | 2 | 1 | | 1 | 2 | 2 | 1 |

**UNIT-I:**

**Introduction to Advanced System Design (ARM Cortex IP):** The ARM RISC design philosophy, System hardware – AMBA bus, System software; ARM registers bank, status registers; vector table, data flow model.

**UNIT-II:**

**Cortex M4 SoC Architecture:** Cortex M SoC Processor: introduction – Block diagram; Interrupts and Processor Reset Sequence.CortexM4

STM32F features; Memory Map; ARM Bus Matrix; Nested Vectored Interrupt Controller (NVIC), Interrupts Vs Exceptions; Cortex M Processor Modes.

**UNIT-III:**

**ARM Instruction Set Architecture (ARM ISA):** Fundamentals of ARM instructions, ARM Assembly instructions: Data processing, Branching, Load-store, SWI and Program Status Register instruction. Thumb ISA.

**UNIT-IV:**

**SoC Programming (STM32F):** GPIO Management: Accessibility & Configurations; Timer Programming; UART: Configuration, baud rate generation, UARTx drivers in C; $I^2C$: Features, modes, Pins and Registers; I2C Driver Programming; SPI: master/slave operation, Pins & Registers; ADC Driver for data sampling & processing needs.

**UNIT-V:**

**ARM Interfacing with Real World:** Interfacing of switches, LEDs; Seven Segment Display; Matrix Keypad; LCD – Design options; DC Motor & Stepper Motor interfacing designs in Embedded C/C++; debugging methods.

**Learning Resources:**

1. ARM System-on-chip Architecture by Steve Furber, Pearson Education, ISBN978-81-317-0840-8, 2E, 2012.
2. STM32 ARM Programming for Embedded Systems, Muhammad Ali Mazidi, Shujen Chen, Eshragh Ghaemi ISBN: 978-099-792-5944, 2018
3. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®-M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Advanced System Design Lab

SYLLABUS FOR B.E. V SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs./week) : 0:0:2 | SEE Marks : 50 | Course Code: **U20PC551EC** |
| Credits : 1 | CIE Marks : 30 | Duration of SEE : 3 Hours |

| COURSE OBJECTIVE | COURSE OUTCOMES |
|---|---|
| 1. Execute ARM assembly programs for data processing needs.<br>2. Design electronic systems with Cortex M4 MCUs<br>3. Design and Realize a System Design using embedded C with ARM Cortex M4 MCU. | On completion of the course, students will be able to<br>1. Implement ARM assembly data processing instructions for Cortex M4.<br>2. Construct programs & Validate designs using cross assembler & compiler.<br>3. Develop embedded C drivers for on-chip peripherals of STM32F411RE.<br>4. Design system level solutions with off-chip components in Proteus<br>5. Realize a complete system using ARM Cortex M4 with different I/Os. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | 1 | 1 | 3 | 2 | 1 |
| CO2 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | 1 | 1 | 3 | 2 | 1 |
| CO3 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | 1 | 1 | 3 | 2 | 1 |
| CO4 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | 1 | 1 | 3 | 2 | 1 |
| CO5 | 3 | 2 | 3 | 2 | 3 | | | | 1 | 1 | 1 | 1 | 3 | 2 | 1 |

## Module – 1 (ARM Cortex M4 Assembly Language Programming)

1. ARM Data formats and Directives.
2. Addressing Modes.
3. Arithmetic & Logical instructions.
4. Looping and Branching Instructions.
5. Conditional Subroutines.
6. ARM Time Delay and instruction pipeline instructions.
7. ARM Conditional Execution of Assembly.

**Module-2 (STM32F4xxx MCU based SBC)**

1. GPIO Programming.
2. Timer Programming.
3. Interfacing 7-segment display.
4. Full duplex UART Driver design in Embedded C.
5. Interfacing a 4x4 Matrix keyboard for input and 2x16 LCD for output.
6. ADC Driver design for interfacing a Sensor.
7. DAC driver design for generating different signals for control system applications.
8. I2C Drivers with STM32F MCU as Master/Slave.
9. SPI Driver design and implementations.

The break-up of CIE:

| | | | |
|---|---|---|---|
| 1. | No. of Internal Test | : | 1 |
| 2. | Max. Marks for internal tests | : | 12 |
| 3. | Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Field Programmable Gate Array (FPGA) Based System Design

SYLLABUS FOR B.E. VI - SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs/Week): 2:0:0 | SEE Marks: 60 | Course Code: **U20PC650EC** |
| Credits: 2 | CIE Marks: 40 | Duration of SEE: 3 Hours |

| COURSE OBJECTIVES | COURSE OUTCOMES |
|---|---|
| The objective of the course is to enable students to apply their knowledge in designing complex digital systems using integrated circuit cells as building blocks and employing hierarchical design methods with the help of EDA tools. Emphasis is given on digital design using Verilog HDL and FPGA architectures | On completion of the course, students will be able to<br>1. Analyse different types of FPGAs and their modules.<br>2. Understand the Project Design using ZYNQ board.<br>3. Design and model combinational circuits with Verilog HDL at different levels.<br>4. Design and analyse various sequential digital circuits by Verilog HDL.<br>5. Develop test benches to system Level Designs. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | | | | | | | | | | | 2 | | |
| CO2 | 2 | 2 | 1 | | | | | | | | | | 2 | | |
| CO3 | 2 | 2 | 1 | | 2 | | | | | | | | 2 | | |
| CO4 | 2 | 2 | 1 | | 2 | | | | | | | | 2 | | |
| CO5 | 2 | 2 | 1 | | 2 | | | | | | | | 2 | | |

**UNIT-I:**

**Introduction to FPGA architecture:** FPGA general description, Different kinds of FPGA packages, FPGA architecture, Internal hard ware modules of FPGA, their meanings and usage, Basic building blocks, Different kinds of I/O modules.

**UNIT-II:**

**FPGA Design Flow:** Zynq Architecture design, Anti fuse, SRAM and EPROM based FPGAs, Project design using Verilog Hardware Description

Language (HDL), Verilog Coding and Simulation of Digital Systems. Implementation examples of Logic functions using LUTs and CLBs.

**UNIT-III:**

**Design & Implementation of Combinational Circuits:** Overview of combinational circuits, Verilog Modelling of Combinational Circuits, Adders, Multipliers, Parity Generator Comparators and implementation of different combinational circuits, High Speed Adders, data path design and Timing issues.

**UNIT-IV:**

**Design & Implementation of Synchronous Sequential Circuits:** Realization of Shift Registers, Realization of a Counter, State diagram, state table, state assignment, choice of flipflops, Timing diagram, One hot encoding, Mealy and Moore state machines, State minimization. FSM based Applications.

**UNIT-V:**

**System Level Design& Implementation:** Introduction to IP Cores, Block Level Design, Implementation of BLOCK RAM, FIFO Design using IP Cores, CPU Sub System Design, Writing Test Benches to Complex Systems.

**Learning Resources:**

1. Pong P Chu, "FPGA Proto Typing by Verilog Examples" WILEY Publications.
2. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
3. Steve Kilts "Advanced FPGA Design: Architecture, Implementation, and Optimization", WILEY Publications.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Field Programmable Gate Array (FPGA) Based System Design Lab

SYLLABUS FOR B.E. VI SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs./week) : 0:0:2 | SEE Marks : 50 | Course Code: **U20PC651EC** |
| Credits : 1 | CIE Marks : 30 | Duration of SEE : 3 Hours |

| COURSE OBJECTIVE | COURSE OUTCOMES |
|---|---|
| The objective of the course is to enable students to apply their knowledge for the design of complex high speed digital circuits and implement them using FPGA. | On completion of the course, students will be able to<br>1. Learn to write HDL code for simulation and synthesis.<br>2. Analyse and understand different combinational and Sequential Circuit examples and use the existing examples for new designs.<br>3. Integration of the above circuits to create a sub system design. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | | | 2 | | | | | | | | 2 | | |
| CO2 | 2 | 2 | | | 2 | | | | | | | | 2 | | |
| CO3 | 2 | 2 | | | 2 | | | | | | | | 2 | | |

**List of Experiments:**

**Getting Started with**

1. FPGA Design Flow using Vivado Tools.
2. Design & Implementation of Combinational Circuits.
3. Design & Implementation of High speed Circuits.
4. Design & Implementation of n-bit Comparator.
5. Design & Verification of Booth Multiplier.
6. Test Bench Creation and Simulation of Synchronous Circuits.
7. Design and Implementation of FSM.
8. Design and Implementation of Block RAM

9. Design and Implementation of FIFO
10. 32 Bit ALU Design Verification with VIO and ILA.
11. Memory Design and Implementation.
12. UART design and Implementation.
13. Mini Project.

**References:** https://reference.digilentinc.com/reference/programmable-logic/zedboard/reference-manual

The break-up of CIE:

| | | | |
|---|---|---|---|
| 1. | No. of Internal Test | : | 1 |
| 2. | Max. Marks for internal tests | : | 12 |
| 3. | Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Design Verification

SYLLABUS FOR B.E. VII – SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs/Week): 2:0:0 | SEE Marks: 60 | Course Code: **U20PC730EC** |
| Credits: 2 | CIE Marks: 40 | Duration of SEE: 3 Hours |

| COURSE OBJECTIVE | COURSE OUTCOMES |
|---|---|
| 1. To provide detailed knowledge in VLSI design process starting from digital design, hardware descriptive languages, synthesis, simulation, verification, FPGA programming & implementation.<br>2. Will understand the entire logic design process and will be able to take the challenges posed by the chip design industry. | On completion of the course, students will be able to<br>1. Write Verilog code, and execute sequential circuits on any VLSI design platform.<br>2. Perform verification and testing.<br>3. Understand and use the System Verilog design and synthesis features.<br>4. Apply the System Verilog verification features including Structures and classes.<br>5. Demonstrate the designs having a set of objective criteria and design constraints. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 1 | 2 | 2 | | | | | | | | | | 2 | 2 | |
| CO2 | 1 | 2 | 2 | | 2 | | | | | | | | 2 | 2 | |
| CO3 | 2 | 2 | 2 | | | | | | | | | | 2 | 2 | |
| CO4 | 1 | 2 | 2 | 2 | | | | | | | | | 2 | 2 | |
| CO5 | 1 | 2 | 2 | 2 | 2 | | | | | | | | 2 | 2 | |

**UNIT-I:**

Blocking and nonblocking assignments in Verilog; Modeling of sequential circuits (Decade Counters, Binary counters, binary sequence detection etc) using Verilog; Writing test benches for these designs; The importance of verification in ASIC design, Functional verification approaches.

**UNIT-II:**

Verification coverage – statement-, block-, branch-, expression-, and FSM-coverage. Verification tools and verification plan; Architecting test benches; Writing basic self-checking test benches; role of tasks and

functions in test benches; automatic taks and functions; Understanding fork-join execution.

**UNIT-III:**
System Verilog as a Hardware Design & Verification Language (HDVL); SV language elements, data types, enumeration types, arrays and dynamic arrays, queues, strings.

**UNIT-IV:**
Structures and classes, SV operators and expressions; Transaction class, Randomization of stimulus; generator class, driver class, scoreboard class, monitor class, checker class; Basic testbench in System Verilog.

**UNIT-V:**
Threads and interprocess communication, Advanced OOP and test bench guidelines, A complete SV test bench.

**Learning Resources:**

1. Verilog HDL: A Guide to Digital Design and Synthesis – by Samir Palnitkar, Prentice Hall PTR Publishers.
2. System Verilog for Verification – a guide to learning the Testbench language features; 2nd edition or 3rd edition– by Chris Spear; Springer Verlag Publications.
3. A System Verilog Primer – by J Bhaskar; BS Publications, India.
4. Writing Testbenches – Functional verification of HDL models; 2nd edition by Janick Bergeron; Kluwer Academic Publishers

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# Design Verification Lab

SYLLABUS FOR B.E. VII SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs./week) : 0:0:2 | SEE Marks : 50 | Course Code: **U20PC731EC** |
| Credits : 1 | CIE Marks : 30 | Duration of SEE : 3 Hours |

| COURSE OBJECTIVE | COURSE OUTCOMES |
|---|---|
| To perform design and verification of different applications of sequential circuits. | On completion of the course, students will be able to<br>1. Design various sequential circuits using HDL.<br>2. Write test benches for the simulation of sequential circuits.<br>3. Verification of design using system Verilog. |

**CO-PO-PSO Mapping:**

| CO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 2 | 2 | 2 | | 3 | | | | | | | | 2 | 2 | |
| CO2 | 2 | 2 | | | 3 | | | | | | | | 2 | 2 | |
| CO3 | 2 | 2 | 2 | | 3 | | | | | | | | 2 | 2 | |

## Laboratory Experiments:

1. Writing Verilog code for sequence detector FSM and running simulation.
2. Verilog coding of the sequence detector using Shift register.
3. Verilog based Design of a decade counter and other special counters.
4. Writing test bench and verifying the working of a Decade Counter.
5. Writing design code in Verilog for a "Candy Vending Machine" problem.
6. Writing test bench using Tasks, and verify the working of the candy vending machine.
7. Measuring the verification coverage of the test bench for Candy Vending Machine.
8. Writing design code for the Washing Machine Controller problem.
9. Writing directed tests in the test bench for Washing Machine Controller and measuring the coverage.

10. Porting the test bench of Candy Vending Machine to System-Verilog (SV) - phase-1.
11. Porting the test bench of Candy Vending Machine to System-Verilog (SV) - phase-2.
12. Measuring verification coverage of the Candy Vending machine Test bench.
13. Porting the test bench of Washing Machine Controller to SV - phase-1
14. Porting the test bench of Washing Machine Controller to SV - phase-2.

The break-up of CIE:

| | | | |
|---|---|---|---|
| 1. | No. of Internal Test | : | 1 |
| 2. | Max. Marks for internal tests | : | 12 |
| 3. | Marks for day-to-day laboratory class work | : | 18 |

Duration of Internal Test: 3 Hours

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# Course Project

SYLLABUS FOR B.E. VII SEMESTER

| | | |
|---|---|---|
| L:T:P (Hrs./week) : 0:0:6 | SEE Marks : 60 | Course Code: **U20PW729EC** |
| Credits : 3 | CIE Marks : 40 | Duration of SEE : 3 Hours |

| COURSE OBJECTIVES | COURSE OUTCOMES |
|---|---|
| Prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design. | On completion of the course, students will be able to<br>1. To select the complex engineering problems beneficial to the industry & society and develop solutions with appropriate considerations.<br>2. To apply modern tools and analyze the results to provide valid conclusions.<br>3. To communicate effectively the solutions with report and presentation following ethics.<br>4. To work in teams and adapt for the advanced technological changes<br>5. To apply management principles to complete the project economically |

**CO-PO/PSO Mapping**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 2 | 3 | 3 | | | 2 | 2 | | | | | | | | |
| CO2 | | | | 3 | 3 | | | | | | | | | | |
| CO3 | | | | | | | | 3 | | 3 | | | | | |
| CO4 | | | | | | | | | 3 | | | 3 | | | |
| CO5 | | | | | | | | | | | 3 | | | | |

**Note:** CO1 & CO2 must be mapped with one of the relevant PSOs based on the domain of the project with 3
CO4 can be mapped to appropriate PSO with level 2

Oral presentation is an important aspect of engineering education. The objective of the course project is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design.

Project topics may be chosen by the student with advice and approval from the faculty members. Students are to be assessed and evaluated as per the following criteria.

- Selection of topic & Literature survey
- Solution & Clarity in Implementation
- Modern tool usage in Implementation
- Results and Analysis
- Team Work, Report writing & Presentation with ethics
- Project Management

**Each student is required to:**

1. Submit a one-page synopsis in the beginning of project work for display on the notice board.
2. Give a 20 minutes presentation through LCD power point presentation followed by a 10 minutes discussion.
3. Submit a report on the project work with list of references and slides used.

Project reviews are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

- Batch size shall be 2 to 3 students.
- Allocation and finalization of the projects by department.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.