VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)

Accredited by NAAC with 'A++' Grade
Ibrahimbagh, Hyderabad-31
Approved by A.I.C.T.E., New Delhi and
Affiliated to Osmania University, Hyderabad-07

Sponsored
by
VASAVI ACADEMY OF EDUCATION
Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR M.E. (ECE)

EMBEDDED SYSTEMS AND VLSI DESIGN (ES&VLSID)

I TO IV SEMESTERS
With effect from 2026-27
(For the batch admitted in 2026-27)
(R-26)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Phones: +91-40-23146040, 23146041
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Institute Vision

Striving for a symbiosis of technological excellence and human values

Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering

Department Mission

To inculcate a spirit of scientific temper and analytical thinking, and train the students in contemporary technologies in Electronics & Communication Engineering to meet the needs of the industry and society with ethical values.

Program Educational Objectives (PEO)

PG – M.E (ES & VLSID) : Embedded Systems and VLSI Design

PEO1: Graduates will be able to design, analyse, and implement systems employing latest techniques and modern tools in the field of Embedded Systems and VLSI Design.

PEO2: Graduates will be able to carry out research independently, write and present a substantial research report.

PEO3: Graduates will be able to demonstrate effective communication skills and leadership qualities with ethical attitudes in broad societal context while working in a multi-disciplinary environment.

Program Outcomes (PO)

PG – M.E (ES & VLSID) : Embedded Systems and VLSI Design :
Graduates will have

PO1: An ability to independently carry out research and development work to offer effective engineering solutions and evaluate system level performance.

PO2: An ability to write and present substantial technical reports.

PO3: An ability to demonstrate in depth knowledge for analysing and solving problems in the area of Embedded Systems and VLSI Design.

PO4: An ability to apply appropriate techniques and modern EDA tools to design and conduct advanced experiments and pursue investigations on circuits and system level design.

PO5: An ability to apply engineering and management principles as a member and leader in a team, to manage projects in multi-disciplinary environment with lifelong learning capabilities.

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DEPARTMENT OF ECE

SCHEME OF INSTRUCTION AND EXAMINATION (R - 26)

M.E - Embedded Systems and VLSI Design (ES&VLSID) FIRST SEMESTER (2026-2027)

M.E - ECE (ES&VLSID) I-Semester								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
		Hours per Week			Duration in Hrs	Maximum Marks		Credits
		L	T	P		SEE	CIE	
THEORY								
P26PC110EC	Professional Core-I: Advanced Embedded System Design	3	-	-	3	60	40	3
P26PC120EC	Professional Core-II: Analog and Digital VLSI Design	3	-	-	3	60	40	3
P26PE1XXEC	Professional Elective - I	3	-	-	3	60	40	3
P26PE1XXEC	Professional Elective - II	3	-	-	3	60	40	3
P26PC140ME	Research Methodology and IPR	2	-	-	3	60	40	2
P26AC110EH	Audit Course-I: English for Research Paper Writing	2	-	-	3	60	40	-
PRACTICALS								
P26PC111EC	Advanced Embedded Systems Laboratory	-	-	4	-	-	50	2
P26PC121EC	Analog and Digital VLSI Design Laboratory	-	-	4	-	-	50	2
	TOTAL	**16**	**-**	**8**	**-**	**360**	**340**	**18**
	GRAND TOTAL	**24**				**700**		

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DEPARTMENT OF ECE

SCHEME OF INSTRUCTION AND EXAMINATION (R - 26)

M.E Embedded Systems and VLSI Design (ES&VLSID) SECOND SEMESTER (2026-2027)

M.E - ECE (ES&VLSID) II-Semester								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
		Hours per Week			Duration in Hrs	Maximum Marks		Credits
		L	T	P		SEE	CIE	
THEORY								
P26PC210EC	Professional Core-III: Embedded Real Time Operating Systems	3	-	-	3	60	40	3
P26PC220EC	Professional Core-IV: VLSI Physical Design	3	-	-	3	60	40	3
P26PE2XXEC	Professional Elective - III	3	-	-	3	60	40	3
P26OE2XXXX	Open Elective	3	-	-	3	60	40	3
P26AC210EH	Audit course-II: Pedagogy Studies	2	-	-	3	60	40	0
PRACTICALS								
P26PC211EC	Embedded System Applications Laboratory	-	-	3	-	-	50	2
P26PC221EC	VLSI Physical Design Laboratory	-	-	3	-	-	50	2
P26PW219EC	Mini Project with Seminar	-	-	2	-	-	50	2
	TOTAL	**14**	**-**	**8**	**-**	**300**	**350**	**18**
	GRAND TOTAL	**22**				**650**		

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DEPARTMENT OF ECE

SCHEME OF INSTRUCTION AND EXAMINATION (R - 26)

M.E Embedded Systems and VLSI Design (ES&VLSID) THIRD SEMESTER (2026-2027)

M.E - ECE (ES&VLSID) III-Semester								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
		Hours per Week			Duration in Hrs	Maximum Marks		Credits
		L	T	P		SEE	CIE	
THEORY								
P26PE3XXEC	Professional Elective – IV	3	-	-	3	60	40	3
P26PE3XXEC	Professional Elective – V	3	-	-	3	60	40	3
PRACTICALS								
P26PW319EC	Dissertation - Phase-I / Internship	-	-	20	-	-	100	10
	TOTAL	**6**	**-**	**20**	**-**	**120**	**180**	**16**
	GRAND TOTAL	**26**				**300**		

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DEPARTMENT OF ECE

SCHEME OF INSTRUCTION AND EXAMINATION (R - 26)

M.E Embedded Systems and VLSI Design (ES&VLSID) FOURTH SEMESTER (2026-2027)

M.E - ECE (ES&VLSID) IV-Semester								
Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			
		Hours per Week			Duration in Hrs	Maximum Marks		Credits
		L	T	P		SEE	CIE	
PRACTICALS								
P26PW419EC	Dissertation – Phase II / Internship	-	-	32	-	Viva – voce (Grade)		16
TOTAL		**-**	**-**	**32**	**-**	**-**	**-**	**16**
GRAND TOTAL		**32**						

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DEPARTMENT OF ECE

Semester	Professional Elective	List of Stream Based Professional Electives (R-26)			
		Professional Elective Stream 1: Embedded Systems		Professional Elective Stream 2: VLSI System Design	
		Course Code	Title	Course Code	Title
I	PE-I	P26PE110EC	Programming Languages for Embedded Systems	P26PE120EC	Advanced CMOS Microfabrication
	PE-II	P26PE130EC	Advanced Computer Organization	P26PE140EC	FPGA Based System Design
				P26PE150EC	Scripting Languages
II	PE-III	P26PE210EC	Hardware-Software Co-Design	P26PE220EC	Design Verification using System Verilog
				P26PE230EC	Static Timing Analysis
III	PE-IV	P26PE310EC	High Level Synthesis	P26PE320EC	Low Power VLSI Design
				P26PE330EC	System on Chip (SoC) Design
	PE-V	P26PE340EC	IoT Architectures and Applications	P26PE350EC	Physical Design Automation
				P26PE360EC	Design for Testability

Audit courses and Open Electives		
S.No.	**Course Code**	**Course Title**
Audit Course – I		
1	P26AC110EH	English for Research Paper Writing
2	P26AC120XX	Value Education
3	P26AC130XX	Stress Management by Yoga
4	P26AC140XX	Sanskrit for Technical Knowledge
Audit Course –II		
1	P26AC210EH	Pedagogy Studies
2	P26AC220XX	Personality Development through Life Enlightenment Skills.
3	P26AC230XX	Constitution of India
4	P26AC240XX	Disaster Management
Open Electives		
1	P26OE210CS	Fundamentals of Python Programming
2	P26OE220XX	Business Analytics
3	P26OE230XX	Industrial Safety
4	P26OE240XX	Operations Research
5	P26OE250XX	Cost Management of Engineering Projects
6	P26OE260XX	Composite Materials
7	P26OE270XX	Waste to Energy

Syllabus for
M.E. ECE (ES & VLSI Design)
I - SEMESTER

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Embedded System Design

Professional Core - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PC110EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Define and Classify an Embedded System along with design issues. 2. Justify the philosophy of ARM core as CPU in SoC designs. 3. Demonstrate ARM ISA Assembly usage for data processing. 4. Implement different I/O interfacing drivers for Cortex M4 MCU in C.	On completion of the course, students will be able to 1. Define, Classify and Analyze embedded system product design with IC Technology. 2. Analyze ARM IP Core usage in design with its programming model and registers. 3. Implement ARM assembly construct for Cortex M4 4. Design device drivers in embedded-C for Cortex M4 to interface different I/O. 5. Propose hardware software codesign issues along with debugging techniques.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	1	2	3	2	-
CO2	1	2	3	2	-
CO3	1	2	3	2	-
CO4	1	2	3	2	-
CO5	1	2	3	2	-

UNIT – I:

Embedded Systems Design Introduction: Definition of Embedded System; Examples; Classifications based on Cost and Size; Hard Real Time Systems, Soft Real Time Systems, Life Cycle of Embedded System. Issues of Time-to-Market; Selection of CPU, memories and I/O; RISC Vs CISC; Design Metric.

UNIT – II:

Embedded systems using ARM: Nomenclature; Core Architecture; Introduction to AMBA Bus; Registers – CPSR, SPSR, Modes; Thumb Mode;

Exceptions, OBD using JTAG; ARM family variants: ARM7, ARM9 and Cortex Cores and comparisons.

UNIT – III:

ARM CortexM4 architecture and Programming: Introduction; Cortex CPU Block diagram; ARM Assembly Level Programming: Load and Store instructions; Data Formats and Directives; Addressing Modes; ALU instructions, Branching instructions.

UNIT – IV:

ARM [STM32F4xx] Real World Interfacing: Interfacing of switches, LEDs; Seven Segment Display; Matrix Keypad interface; LCD interfacing; DC Motor, Stepper Motor interfacing designs.

UNIT – V:

Hardware Software Codesign: Co-Design with a case study of Adaptive Cruise Control Design. Software architectures–Round Robin, RR with interrupts, Functional Queue.

Debugging: Host, Target, Big-Endian, Little-Endian ISA. Debugging methods in S/W & H/W.

Learning Resources:

1. STM32 ARM Programming for Embedded Systems, Muhammad Ali Mazidi, Shujen Chen, Eshragh Ghaemi ISBN: 978-099-792-5944, 2018
2. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®-M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC
3. NPTEL-"Embedded System Design Using ARM", https://archive.nptel.ac.in/courses/106/105/106105193/

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Analog and Digital VLSI Design

Professional Core - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PC120EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Analyse the effect of sizing the devices of CMOS circuits and its performance in terms of logical and electrical efforts. 2. Introduce the principles of analog circuits and apply the techniques for the design of analog integrated circuit	On completion of the course, students will be able to 1. Design MOS transistor circuits. 2. Know the Physical design flow and different modelling design. 3. Design sequential circuits at higher level. 4. Design analog circuits like single stage and differential amplifiers. 5. Analyze frequency response of active circuits.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2		1		
CO2	1		1		
CO3	2		3		
CO4	2		3		
CO5	2		2		

UNIT – I:

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, Delay, Wire delay models. Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model.

UNIT – II:

Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, transmission gate logic.

UNIT – III:

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, and Non-bistable sequential circuit.

Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, and TFET.

UNIT – IV:

Single Stage Amplifier: CS stage with resistance load, Diode connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascode stage, Choice of device models. Differential Amplifiers: Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT – V:

Current mirrors: Basic current mirrors, Applications of current Sources, Sizing issues, Cascode mirrors, Active current mirrors.

Learning References:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
5. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition.
6. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Programming Languages for Embedded Systems

Professional Elective - I

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE110EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To impart knowledge on embedded C 2. To understand algorithms in C++. 3. To Develops CPP programming. 4. To understand Inheritance and overloading 5. To acquire the knowledge about templates concepts.	On completion of the course, students will be able to 1. Write an embedded C application of moderate complexity. 2. Develop and analyze algorithms in C++. 3. Design embedded software using object oriented programming principles. 4. Apply the concept of generic programming for embedded systems. 5. Write exception handlers for embedded software.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			3	2	
CO2			3	3	
CO3			2	3	
CO4			2	2	
CO5			3	2	

UNIT – I

Embedded 'C' Programming
- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT – II

Object Oriented Programming - Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural

programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT – III

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT - IV

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT – V

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Learning Resources:

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011
3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

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3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced CMOS Microfabrication

(Professional Elective-I)
SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26PE120EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To introduce the fundamental concepts of semiconductor physics and materials essential for IC fabrication. 2. To familiarize with thermal oxidation and thin-film deposition processes used in CMOS technology. 3. To understand key microfabrication steps such as diffusion, ion implantation, photolithography, and etching. 4. To explore the complete CMOS and FinFET fabrication processes and address associated technological challenges. 5. To impart knowledge of characterization methods used to analyze semiconductor material and device properties.	On completion of the course, students will be able to 1. Understand fundamental semiconductor properties, carrier dynamics, and materials relevant to microfabrication. 2. Apply oxidation and thin-film deposition techniques used in CMOS process technology. 3. Demonstrate knowledge of diffusion, ion implantation, photolithography, and etching in microfabrication. 4. Analyze CMOS and FinFET fabrication flows, including advanced techniques like salicidation and damascene processing. 5. Utilize electrical and physical characterization tools for evaluating semiconductor devices and materials.

CO-PO/PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2		2		
CO2	3		3		
CO3	3		3		
CO4	3		3		
CO5	2		2		

UNIT-I :

FUNDAMENTALS OF SEMICONDUCTORS: Crystal lattices, Bulk crystal Growth, Epitaxial Growth, Bonding forces and energy bands in solids, Charge carriers in semiconductors, Carrier concentrations, Drift of carriers in Electric and Magnetic Fields, Hall effect, Fermi level at equilibrium, Intrinsic vs Extrinsic semiconductors, Excess carriers in semiconductors, Diffusion and recombination, Diffusion length, Properties of Silicon and compounds, Gallium Arsenide, Metals used in IC fabrication.

UNIT-II:

FABRICATION TECHNIQUES I: Top-Down and Bottom-Up Approach, Wafer Cleaning, Silicon Oxidation Techniques: Thermal Oxidation process, Deal-Groove model of oxidation, types of oxidation techniques, growth mechanism, factors affecting the growth mechanisms, dry & wet oxidation. Film deposition: Chemical Vapour deposition, Physical Vapour deposition, Polysilicon deposition, Dielectric deposition.

UNIT-III:

FABRICATION TECHNIQUES II: Diffusion: Basic diffusion process, Extrinsic diffusion, Lateral diffusion, Ion Implantation: Range of Implanted Ions, Implant damage and Annealing, Tilt- Angle Ion Implantation. Photolithography: Optical lithography, Photoresists, Masks, Pattern Transfer. Etching: Wet Chemical Etching, Dry Etching, Isotropic and Anisotropic etching.

UNIT-IV:

CMOS FinFET: Basic MOS Capacitor, MOSFET fabrication process, CMOS Technology, Challenges of STI versus LOCOS, FinFET architecture, Gate first versus gate last, contact resistance issues of simple metal-silicon contact, metal silicides, salicidation, evolution from Ti to Co to Ni silicide, Damascene and dual-Damascene process.

UNIT-V:

CHARACTERIZATION TECHNIQUES: Resistivity: Two-Point versus Four-Point Probe, Carrier and doping density: Capacitance-Voltage (C-V) characterization, Current-Voltage characterization, Optical characterization: Introduction to Ellipsometry, Scanning probe microscopy: SEM, TEM and AFM.

Learning Resources:

1. Ben Streetman, Sanjay Banerjee - Solid State Electronic Devices-Prentice Hall (2006)
2. Jan M. Rabaey, Anantha Chandrakasan, Digital Integrated Circuits: A Design Perspective, Prentice Hall of India, 2016.
3. Tai-Ran Hsu - MEMS & Microsystems Design and Manufacture-Tata McGraw-Hill Education (2002).
4. Weste, Neil H E_Harris, David Money - CMOS VLSI Design_ A Circuits and Systems Perspective-Addison-Wesley (2010).
5. Stephen D. Senturia, Microsystem design, Springer (India), 2006.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Computer Organization

Professional Elective - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE130EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
By the end of this course, students should be able to 1. Understand RISC-V as an open ISA, comparing its modularity and extensibility with proprietary architectures (ARM, x86). 2. Analyze RISC-V's instruction formats, base and standard extensions. 3. Design pipelined RISC-V systems, addressing hazards, branch penalties, and superscalar techniques for performance optimization. 4. Evaluate privileged ISA features and custom extensions for tailored hardware/software solutions. 5. Apply parallel computing concepts (ILP, multiprocessors, SIMD) to RISC-V-based systems, including shared memory and vector processors.	On completion of the course, students will be able to 1. Compare RISC-V's open-standard advantages with ARM/x86 and justify its use cases in modern computing. 2. Write and debug RISC-V programs using base and extended ISAs 3. Optimize RISC-V pipeline performance by mitigating hazards and implementing superscalar techniques. 4. Configure RISC-V's privileged modes for interrupt handling. 5. Design scalable RISC-V systems leveraging parallelism (multicore, SIMD, vector processors) for high-performance applications.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	3		
CO2	2	1	3	2	
CO3	3	1	3	2	
CO4	3	1	3	1	
CO5	3	1	3		
CO6	2	1	3		

UNIT-I: Introduction to RISC-V

Motivation: Why RISC-V?, Open ISA vs. Proprietary ISAs (ARM, x86), Key Features of RISC-V like Modularity, Extensibility, etc., Open ISA vs. Proprietary ISAs (ARM, x86), Comparison with Other Architectures : ARM vs. RISC-V vs. x86

UNIT-II: RISC-V ISA Basics
Instruction Formats & Types: R-Type, I-Type, S-Type, B-Type, U-Type, J-Type, Base Integer ISA (RV32I, RV64I), Registers (x0-x31, Zero Register), Arithmetic, Logical, and Control Instructions, Memory Access (Load/Store)

UNIT-III: Advanced RISC-V ISA Extensions
Standard Extensions: M (Multiplication & Division), A (Atomic Operations), F (Single-Precision Floating Point), D (Double-Precision Floating Point),C (Compressed Instructions), Privileged ISA (Supervisor & Machine Mode): CSRs (Control & Status Registers),Exceptions, Interrupts, and Traps, Custom Extensions: How to Define Custom Instructions

UNIT-IV: Pipelining Techniques
Super Scalar techniques, Super scalar and super pipeline design, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

UNIT-V: Parallel Computer Systems
Instruction Level Parallelism (ILP), Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors, SIMD computers and Super computers

Learning Resources:

1. The RISC-V Reader: An Open Architecture Atlas, David Patterson, Andrew Waterman, Strawberry Canyon LLC.
2. John L. Hennessy and David A. Patterson, Computer Architecture – A quantitative Approach, 3rd Edition, Elsevier, 2005.
3. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
4. "Programming with RISC-V", Steve Rhoads

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FPGA Based System Design

Professional Elective - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE140EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
By the end of this course, students will be able to: 1. Develop fundamental understanding of RTL design methodology and hardware description using Verilog HDL. 2. Develop skills in designing combinational and sequential digital circuits using synthesizable Verilog RTL. 3. Develop proficiency in RTL simulation, testbench development, waveform analysis and functional debugging. 4. Introduce FPGA architecture, Vivado design flow, synthesis, constraints, implementation and timing analysis. 5. Design, simulate and implement a complete FPGA-based digital system.	After completing this course, students will be able to: 1. Understand and describe RTL design concepts, Verilog HDL constructs, FPGA architecture and programmable logic resources. 2. Develop synthesizable Verilog RTL models for combinational and sequential digital systems. 3. Design and verify FSMs, memories, FIFOs and digital communication interfaces using Verilog and simulation testbenches. 4. Analyze and evaluate RTL designs using Vivado elaboration, simulation, synthesis reports, resource utilization and timing analysis. 5. Design and implement an FPGA-based digital system through the complete RTL-to-bitstream design flow.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	3		
CO2	2	1	3		
CO3	2	1	3	2	
CO4	2	1	3	3	
CO5	3	1	3	2	

UNIT - I:

Introduction to RTL Design: Register Transfer Level abstraction, RTL versus gate-level design, RTL versus software programming, Combinational RTL, Sequential RTL, Hardware-oriented design thinking, RTL design methodology, Introduction to Vivado Design Flow

UNIT - II:

Combinational and Sequential RTL: Data-flow modeling, Behavioral modeling, if-else, case, Nested conditional statements, Arithmetic circuits, Logic

circuits, case study on ALU design, Flip-flop modeling, Clocked always blocks., Registers, Counters

UNIT – III:

RTL Simulation and Verification: Simulation versus synthesis, RTL simulation flow, Behavioral simulation, Testbench architecture, Design Under Test (DUT), Stimulus generation, Simulation time, $display, $monitor, $finish, Waveform analysis, Debugging RTL, Verilog Testbenches: Testbench structure, DUT instantiation, Test vectors, Self-checking testbench, Expected versus actual output, Functional verification, Finite State Machines : State diagram, State table, State assignment, Mealy machine, Moore machine, One-hot encoding, Timing diagram, FSM Applications : Sequence detector, Elevator controller

UNIT - IV:

FPGA Architecture and Technologies: Introduction to Simple Programmable Logic Devices (SPLDs), CPLDs, FPGA architecture elements: Configurable Logic Blocks (CLBs), Look-Up Tables (LUTs),Programmable interconnects, I/O blocks, Block RAM, DSP resources, Clock management resources, FPGA Technologies : SRAM-based FPGA, Antifuse FPGA, EPROM-based FPGA, Comparison of FPGA technologies, FPGA versus ASIC

UNIT -V:

FPGA Implementation and Timing analysis: Xilinx Design Constraints (XDC) , Pin assignments, I/O standards, Clock constraints, Timing constraints, Input/output delay constraints, Synthesis : RTL-to-netlist conversion, Technology mapping, FPGA resource mapping, Resource utilization and Synthesis reports, Timing analysis , Setup time , Hold time , Slack, Maximum operating frequency, Timing closure, FPGA Programming: Bitstream generation, Hardware Manager, FPGA configuration, Programming the FPGA , Hardware testing and Debugging

Learning Resources:

1. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Pearson Education 2009.
2. Wayne Wolf, FPGA based System Design, Pearson Education 2009.
3. Steve Kilts, Advanced FPGA Design: Architecture, Implementation and optimization, A Jhon Wiley & Sons, Inc., publication.
4. Pong P Chu, "FPGA Proto Typing by Verilog Examples" WILEY Publications.
5. Data sheets and Manuals from Xilinx, Altera, AMD, Actel.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Scripting Languages

Professional Elective - II

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE150EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To understand control structures of perl. 2. To classify character classes. 3. To apply subroutines and data structures. 4. To acquire the knowledge extending perl. 5. To understand broad features of SKILL, CGI.	On completion of the course, students will be able to 1. Design control structures of perl. 2. Apply subroutines and data structures. 3. Extend perl to embedding perl. 4. Classify character classes. 5. Model features of SKILL, CGI.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			2		1
CO2			2		1
CO3			2		1
CO4			2		1
CO5			2		

UNIT – I

Overview of scripting languages-PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT – II

Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT – III

Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions.
Inter process communication,- signals, files, pipes, sockets,.

UNIT – IV

Threads- process model, thread model, Perl debugger- using debugger commands, customization, internals and externals, internal data types, extending Perl, embedding Perl, exercises for programming using Perl.

UNIT – V

Other languages: Broad features of other scripting languages SKILL, CGI, java script, VB script.

Learning Resources:

1. Larry Wall, Tom Christiansen, John Orwant, "programming perl", oreilly publications, 3rd edition.
2. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly publications.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (Autonomous)
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DEPARTMENT OF MECHANICAL ENGINEERING

Research Methodology and IPR

SYLLABUS FOR M.E. - I SEMESTER

L:T:P (Hrs./week) : 2:0:0	SEE Marks : 60	Course Code: **P26PC140ME**
Credits : 2	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The objectives of this course are to: 1. Learn the research methodology and formulation. 2. Know the sources of literature, method for collection of research data and report writing. 3. understand IPR laws and Acts.	On completion of the course, the student will be able to: 1. List various types of research and explain its significance in the relevant field. 2. review the relevant literature and summarize information for formulating the research problem. 3. generate, analyze and organize the data for the preparation of research report. 4. explain different types of intellectual property rights and its related laws. 5. discuss the patent administration system and patenting procedure.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	2	1		1
CO2	2	2	1		1
CO3	2	2	1		1
CO4	2	2	1		1
CO5	2	2	1		1

UNIT - I

Research Methodology: Meaning of research, Objectives and motivation of research, types of research, research approaches, significance of research, research methods versus methodology, criteria of good research, Research problem formulation.

UNIT - II

Literature survey: Importance of literature survey, sources of information, Literature review: Need of Literature review, Plagiarism, research ethics, errors in research, Assessment of quality of journals.

UNIT - III

Data collection & report preparation: Collection of primary data, secondary data, data organization, methods of data grouping, diagrammatic

representation of data, graphic representation of data. Effective technical writing and how to write report, format of a research proposal, contents of a standard technical journal/conference paper, contents of dissertation.

UNIT - IV

Introduction to Intellectual property law: Basics and types of intellectual property, international organizations, agencies and treaties.

Law of Trademarks: Purpose and functions of trademarks, types of Marks, acquisition of trade mark rights, protectable matter and trade mark registration process, Trade Mark Act.

UNIT - V

Law of copyrights: Introduction, common law rights. Rights of reproduction, rights to display work publicly, other limitations of exclusive rights, copyright ownership issues, copy right registration and Berne convention.

Law of Patents: Administration of Indian patent system, Introduction, rights under patent law. Design patents, Plant patents. Patenting process. Patent ownership and transfer, new developments in IPR and international patent laws, Geographical Indications.

Learning References:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'.
2. C. R. Kothari-Research Methodology Methods and Techniques, Second revised edition, New Age International (P) limited Publishers, New Delhi.2013.
3. Ranjit kumar, Research methodology, A step-by-step Guide for Beginners, second Edition, Sage Publications India Pvt Ltd, New Delhi.2017.
4. Panneer Selvam, Research Methodology, Second Edition, PHI Learning Pvt Ltd, New Delhi.
5. Deborah E. Bouchoux -Intellectual Property, the law of trademarks, Copyrights, Patents and Trade Secrets. Fourth Edition, CENGAGE Learning India private Limited, New Delhi.2013.
6. P. Narayana, Intellectual property law, Third Edition, Eastern Law House, New Delhi.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF HUMANITIES AND SOCIAL SCIENCES

English for Research Paper Writing

Audit Course - I

SYLLABUS FOR M.E. - I SEMESTER

L:T:P (Hrs./week) : 2:0:0	SEE Marks : 60	Course Code: **P26AC110EH**
Credits : -	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The course will enable the learners to: 1. Understand, how to improve writing skills and level of readability. 2 Learn about what to write in each section. 3 Understand the skills needed when writing a Title 4 Ensure the good quality of paper at very first-time submission	1. Apply the principles of academic writing to create clear, concise, coherent, and well-structured paragraphs and documents. 2. Demonstrate ethical and effective research communication through paraphrasing, proper citation practices, and the presentation of research findings. 3. Organize and develop the major sections of a research paper, including literature review, methodology, results, discussion, and conclusions. 4. Construct impactful research paper components such as titles, abstracts, introductions, and literature reviews using appropriate academic conventions and writing strategies. 5. Prepare a complete research manuscript by effectively writing methods, results, discussions, and conclusions while ensuring quality and readiness for publication.

UNIT-I: Foundations of Academic Writing

Planning and Preparation, Word Order, Breaking up long sentences. Structuring Paragraphs and Sentences, Being concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II: Presenting Research Effectively

Clarifying Who Did What, Highlighting your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT-III: Structuring the Research Paper

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV: Crafting Impactful Research Components (Part I)

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, useful phrases, how to ensure paper is as good as it could possibly be the first-time submission.

UNIT-V: Crafting Impactful Research Components (Part II)

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

METHODOLOGY ASSESSMENTS

- Case Studies
- Demonstration
- Online assignments
- Individual and Group
- Presentations
- Expert lectures
- Writing and Audio-visual lessons

Learning Resources :

learn.talentsprint.com

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

The break-up of CIE: Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Embedded Systems Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 0:0:4	SEE Marks : -	Course Code:**P26PC111EC**
Credits : 2	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
1. Design Embedded Systems by using ARM Cortex M4x based MCU as the CPU. 2. Implement real world interfacing with ARM and design prototypes.	On completion of the course, students will be able to 1. Program ARM based microcontroller using its assembly constructs. 2. Implement C constructs to design ARM based embedded system. 3. Interface real world input and output devices to ARM 4. Design and execute a mini project for the given specifications. 5. Propose different debugging methods for implementing embedded systems.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5
CO1	1	2	3	2	-
CO2	1	2	3	2	-
CO3	1	2	3	2	-
CO4	1	2	3	2	-
CO5	1	2	3	2	-

List of Experiments using Embedded C/Embedded C++:

Module – 1 (ARM Cortex M4 Assembly Language Programming)

1. ARM Data formats and Directives.
2. Addressing Modes.
3. Arithmetic & Logical instructions
4. Looping and Branching Instructions
5. Conditional Subroutines
6. ARM Conditional Execution in Assembly

Module-2 (STM32F4xxx MCU based SBC)

7. GPIO Programming
8. Interfacing 7-segment display.
9. Interfacing a 4x4 Matrix keyboard for input and 2x16 LCD for output.
10. Developing user interface for ARM.
11. Timer Programming
12. Full duplex UART Driver design in Embedded C.

Suggested tools for used:

1. Hardware Target CPU; STM32F4xx (ARM CortexM4F from ST.
2. Embedded Compiler – Keil µVision5 IDE: ARM compiler
3. Embedded Debugger – Keil µVision5 Debugger
4. Hardware Simulator – Proteus 8.x

The break-up of CIE :

1. No. of Internal Test	:	1
2. Max. Marks for each internal tests	:	20
3. Marks for assessment for day to day evaluation	:	30

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Analog and Digital VLSI Design Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - I SEMESTER

L:T:P (Hrs./week) : 0:0:4	SEE Marks : -	Course Code:**P26PC121EC**
Credits : 2	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
1. To demonstrate computer aided design tools for the modeling, design, analysis and verification of digital and analog integrated circuits.	On completion of the course, students will be able to 1. Develop HDL code for combinational and sequential logic circuits and Synthesize them. 2. Verify the designs using system Verilog. 3. Design and simulate analog circuits.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	3	3	-
CO2	3	-	3	3	-
CO3	3	-	3	3	-

Part A

1. Design and simulate Adder /Counter using Verilog HDL.
2. ASIC Synthesis of Adder/ Counter and find its performance parameters.
3. Design and Simulate a traffic signal controller using finite state machine.
4. Verify functionality of adder with test bench using System Verilog.
5. Verify functionality of Counter with test bench using System Verilog.
6. Insert clock gating for power optimization in Counter.
   Note: Above experiments are to be carried out using Cadence tools (incisive simulator and genus)

PART B

7. Design and Simulation of Symmetrical CMOS inverter and evaluate its performance.
8. Design and simulate a 6-T SRAM cell and find its parameters.
9. Design and simulation of current mirror and plot its behavior.

10. Simulate a single stage MOS amplifier with two different loads and compare their performance.
11. Design and Simulate a differential amplifier with active load.
12. Design and simulate a general purpose CMOS OPAMP.

Note: Above experiments are to be carried out using Cadence tools (virtuoso Schematic composer and spectre circuit simulator)

Note: Minimum of ten experiments are to be conducted.

The break-up of CIE :

1.	No. of Internal Test	:	1
2.	Max. Marks for each internal tests	:	20
3.	Marks for assessment for day to day evaluation	:	30

Duration of Internal Test : 3 Hours

Syllabus for
M.E. ECE (ES & VLSI Design)
II - SEMESTER

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded Real Time Operating Systems

Professional Core - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PC210EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Understand the fundamentals of RTOS 2. Study the task management and scheduling algorithms 3. Explore the Linux kernel structure and its process management 4. Understand the various device drivers and debugging techniques in Linux 5. Apply RTOS concepts in industry-relevant case studies	On completion of the course, students will be able to 1. Differentiate OS, RTOS and classify Real-Time kernels. 2. Demonstrate the use of different scheduling algorithms to estimate the deadline and propose different inter-task-communication models opted in RTOS. 3. Describe Linux kernel architecture and process management. 4. Differentiate Linux user space processes and kernel space threads and implement device drivers using Shell APIs. 5. Suggest fault tolerance methods for real time systems

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2		
CO2	2	2	1		
CO3	2	2	1		
CO4	3	2	2	1	1
CO5	1	1	2	1	1

UNIT–I

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS; Architecture of RTOS, Kernels – classifications, importance of scheduler in OS: objectives and functions; Hard versus Soft Real-time systems – examples, Jobs & Processes, timing constraints. Pre-emptive Vs Non-pre-emptive kernels.

UNIT-II

Task Priorities, Scheduling, inter task Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section: Re- entrant Functions, Inter Process Communication (IPC) – IPC

through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.
Scheduling Algorithms – RMS, Preemptive EDF scheduling – principle, comparisons.

UNIT-III

Linux Kernel 2.x architecture – File system, Concepts of Process – creation, Process Control Block (PCB); process Vs thread; Concurrent Execution. Process Management in Linux–forks Vs Vfork; process state transitions, zombie state, Memory Management Algorithms.

UNIT-IV

Device Drivers & Communication with Hardware – Definition; advantages of Modules; kernel space Vs user space; Concurrency and Race Conditions; classification of device drivers – character drivers, block drivers and net drivers, Interrupt handling in RTOS, Debugging Techniques.

UNIT-V

Fault-Tolerance Techniques & RTOS Application Domains: What causes failures, Fault types, Fault detection, Hardware and software Redundancy. Case studies of RTOS-RTOS for Image Processing – Embedded RTOS for AI and ML applications – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Learning Resources:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-to- Use Modules in C", CMP Publishers Jan 1999.
2. Robert Love, "Linux Kernel Development" (3rd Edition), Novell Press 2010.
3. Jane W.S. Liu, Real Time Systems, Pearson Education, Asia, 2001.
4. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, "Linux Device Drivers", 3rd Edition, O'Reilly Media Publishers
5. Real Time Systems, C.M. Krishna and G. Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Physical Design

Professional Core - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PC220EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To understand the structures of different components of VLSI design. 2. To draw stick and layout diagrams of circuits. 3. To acquire the knowledge of cell based designs.	On completion of the course, students will be able to 1. Design the structures of different components of VLSI design. 2. Apply the basic concepts of physical design to layouts and stick diagrams. 3. Apply Design rules for layouts of circuits. 4. Design hierarchical circuit Layouts using cell concepts. 5. Analyze the basic algorithms which are involved in the process of physical design automation.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1				2	
CO2				2	
CO3			1	3	
CO4				3	
CO5	1			2	

UNIT – I

VLSI Design cycles and new trends in Design cycles, physical design cycles and new trends in physical design cycles, Components of VLSI, Various layers of VLSI, Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors ,Brief review of technology , cost and performance analysis.(Reference 1)

UNIT – II

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects), physical design of logic gates – NOT, NAND and NOR. Mask overlays for different structures. Parasitics – latch up and its prevention. Device matching and common centroid techniques for analog circuits(Reference 1 and 3)

UNIT – III

Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect

on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams. (Reference 4)

UNIT – IV

Cell concepts – cell based layout design – Wein-berger image array — design hierarchies. System level physical design- large scale physical design , interconnect delay modeling,cross talk, floor planning, routing and clock distribution.(Reference1 and 3)

UNIT – V

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): Basic terminology,graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms. (Referene 1 and 2)

Learning Resources:

1. Algorithms for VLSI Physical Design automation, Naveed Sherwani.3rd edition Kluwer academic publishers
2. Algorithms for VLSI Design automation, Sabith H.Gerez ,John Wiley & sons, Inc.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
4. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
5. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Hardware-Software Co-design

Professional Elective - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE210EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To understand architectures, co-design methodology and design	On completion of the course, students will be able to 1. Identify the need for co-design 2. Model data flow and implement the same through software and hardware 3. Construct data flow and control flow graphs 4. Design data flow model for a FSM 5. Design an SoC for given application

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages, Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Learning Resources:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design Verification using System Verilog

Professional Elective - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE220EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To introduce the fundamentals of hardware design verification and the role of SystemVerilog as a verification language. 2. To develop understanding of SystemVerilog data types, procedural constructs, and advanced data structures used in verification environments. 3. To explain object-oriented programming concepts in SystemVerilog and their application in reusable verification components. 4. To enable students to design and implement SystemVerilog-based verification testbenches using randomization, constraints, and inter process communication. 5. To familiarize students with modern verification methodologies such as UVM and apply them to verify digital designs like FIFO and ALU.	On completion of the course, students will be able to 1 Explain the hardware verification process and apply SystemVerilog data types and data structures for verification environments. 2 Apply advanced concepts such as procedural statements, tasks, functions, and parallel constructs in SystemVerilog to implement verification of combinational circuits. 3 Apply object-oriented programming concepts such as classes, inheritance, polymorphism, and virtual interfaces to build reusable verification components to verify sequential circuits. 4 Develop SystemVerilog testbenches with constrained random stimulus, generators, drivers, monitors, and assertions to verify simple protocols. 5 Design and implement UVM-based verification environments and verify FIFO and ALU.

CO-PO Mapping:

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	3	1	–
CO2	2	1	3	2	–
CO3	2	1	3	2	1
CO4	3	1	3	3	1
CO5	3	2	3	3	3

UNIT - I

SystemVerilog Fundamentals for Verification: Introduction to Hardware Verification, Need for Verification, Simulation vs Verification Flow, Overview of SystemVerilog for Design and Verification, SystemVerilog Data Types:2-State and 4-State Data Types, Built-in Data Types (bit, logic, int, byte, shortint, longint),Net Types (wire, tri),Packed and Unpacked Arrays, Fixed-Size Arrays, User Defined Types: typedef, Enumerated Types, Structures and Unions, Other Data Types: Constants, Strings,

Expression Width Rules, Advanced Data Structures : Dynamic Arrays, Queues, Associative Arrays.

UNIT - II

Advanced concepts of SystemVerilog for verification: Procedural Blocks (initial, always), Conditional Statements, Looping Constructs, Tasks and Functions: Tasks, Functions, Void Functions, Routine Arguments, Local Data Storage, Time Values, Parallel Processing: fork…join, fork…join_any, fork…join_none, Inter process Communication: Mailbox, Semaphore, Events.

UNIT – III

Object-Oriented Programming Concepts for Verification: Introduction to Object-Oriented Programming in Verification, Classes and Objects: Class Definition, Creating Objects, Constructors, Object Deallocation, Class Members: Properties, Methods, Static Variables, Encapsulation: Public vs Private Members, Scoping Rules, Class Routines: Defining Functions and Tasks in Classes, Defining Routines Outside the Class, Advanced OOP Concepts: Inheritance, Polymorphism, Virtual Methods, Abstract Classes
Virtual Interfaces: Need for Virtual Interfaces, Using Interfaces in Classes.

UNIT - IV

Testbench Architecture and Verification Methodology: Verification Process and Verification Planning, Building a Simple Testbench: Transaction Class, Generator, Driver, Monitor, Randomization and Constraint-Based Verification: Introduction to Constrained Random Verification, Randomization Basics: rand and randc variables, Randomization Functions, Constraints: Constraint Blocks, Constraint Solving, Valid Constraints, Interfaces, Assertions and DUT Connectivity: Connecting the Testbench with Design Under Test (DUT).

UNIT - V

Introduction to Universal Verification Methodology (UVM): Overview of Verification Methodologies, Need for Standard Verification Methodology, UVM Architecture, UVM Testbench Components, Case Study: Verification of a FIFO, Verification of ALU.

Learning Resources:

1. A System Verilog Primer – by J Bhaskar; BS Publications, India.
2. Chris Spear Synopsys, Inc. "SystemVerilog for Verification A Guide to Learning the Testbench Language Features" Springer.
3. Janick Bergeron, Writing Testbenches Using SystemVerilog, Springer.
4. Ray Salemi, The UVM Primer, Doulos/Verification training publisher.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Tests	: 30
2. No. of Assignments	: 3	Max. Marks for each Assignment	: 5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	: 5

Duration of Internal Tests: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Static Timing Analysis

Professional Elective - III

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE230EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will 1 understand clock domains and critical paths in a given logic design 2 Interpret extracted parasitics and reduce parasitics in critical paths 3 Estimate the Interconnect delays and calculate multiple path slacks 4 Perform cross-talk and Noise analysis in a given net 5 Perform timing analysis and verification across multicycle paths and clock domains	On completion of the course, students will be able to 1. Identify critical paths and estimate propagation delays and skews in a given data-path (PO1 and PO2) 2. Compare the performance of Elmore delay model and higher order interconnect delay models (PO3) 3. Analyse Cross-talk Noise and its reduction in a given data path (PO2) 4. Perform timing analysis across multicycle paths and interpret the results (PO2, PO5) 5. Estimate the timing across multiple clock domains and refine the timing by path balancing (PO2, PO3 and PO5)

UNIT – I:

STA Concepts : CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions.

UNIT – II:

Interconnect Parasitics: RLC for Interconnect, T-model, Pi-model, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets.

UNIT – III:

Delay Calculations: Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging , Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation , Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths Slack Calculation.

UNIT – IV:

Crosstalk and Noise Analysis: Crosstalk Glitch Analysis, Basics Types of Glitches, Rise and Fall Glitches, Overshoot and Undershoot Glitches, Glitch Thresholds and Propagation, DC Thresholds, AC Thresholds, Noise Accumulation with Multiple Aggressors, Aggressor Timing Correlation, Aggressor Functional Correlation, Crosstalk Delay Analysis, Basics, Positive and Negative Crosstalk, Accumulation with Multiple Aggressors, Aggressor Victim Timing Correlation, Aggressor Victim Functional Correlation, Timing Verification Using Crosstalk Delay, Setup Analysis, Hold Analysis, Computational Complexity, Hierarchical Design and Analysis, Filtering of Coupling Capacitances, Noise Avoidance Techniques.

UNIT – V:

STA Environment & Timing Verification : What is the STA Environment, timing issues, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Constraining Output Paths, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Multicycle Paths, Crossing Clock Domains, False Paths, Half-Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Examples, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks.

Learning Resources:

1. J. Bhasker, Rakesh Chadha "Static Timing Analysis for Nanometer Designs A Practical Approach" springer, 2009.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEAPRTMENT OF HUMANITIES AND SOCIAL SCIENCES

Pedagogy Studies

Audit Course - II

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 2:0:0	SEE Marks : 60	Course Code: **P26AC210EH**
Credits : -	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Objectives of this course are to get students: 1. Understand and identify different behavioural styles and adapt training as necessary. 2. Identify the characteristics of an exceptional facilitator 3. Understand and identify different behavioural styles and adapt training as necessary. 4. Understand how to make lecture-based programs active. 5. Make effective trainer aids such as power points and learn to identify all the dependencies	Upon the completion of this course the students will be expected to: 1. Do a Learning Style inventory and understand theirs, and their students' learning style 2. Demonstrate successful understanding of key concepts during a practice presentation. 3. Do a need analysis and why it is a necessary step in any training program. 4. Develop strategies for different types of learners, handling hecklers, bullies, and other disruptive participants 5. Present information in a clear, concise, engaging manner.

From Fabulous to Fantastic -The Art and Science of Teaching the Digital Generation

Keeping information fresh and reinforcing new learning is a constant challenge for an instructor imparting knowledge to an adult. How do you choose activities that are fun but meaningful? How do you assess the level of knowledge already in the room? Is there a formula for creating a successful learning session?

This course is designed to nurture the process of learning, to facilitate sharing of field level experience and giving constructive feedback on training style and delivery. This Audit Course will teach participants how to determine the needs of an audience, improve classroom charisma, handle difficult participants, use activities effectively, and more.

Course Outline

UNIT-1 - Astounding Adults: How they learn

Teaching adults calls for trustworthiness and neutrality while keeping the discussion focused. The first two sessions are about how adults learn how to help in retention and recall.

- How do adults learn
- Pedagogy and Andrago
- Malcolm Knowles theory of Andragogy
- Neuro Linguistic programming
- Kolb's learning styles
- Helping adults learn

UNIT-2 - Classic Course/Class Design

This section's focus is on creating a classic course design that is tailor made for the trainee's learning style. This section also focuses on assessing the trainees' needs in class and customizes activities/direct discussions to address these needs. This section is delivered in two sessions.

- Six thinking hats and the classic course design
- Creating a beautiful body
- Opening
- Main body
- Grand finale

Unit 3 -Beating Murphy's Law

This section is designed to help trainers make effective trainer aids such as power points and learn to identify all the dependencies in advance and have sufficient back up plans, in case there are technical issues. This section is spread over four sessions.

- Power Point
- The Rule of Three
- Anecdotes and Metaphors
- Beat Murphy's Law
- Awesome audiovisuals

Unit 4 - Dazzling Deliveries

Keeping trainees focused so they can get their desired results takes skill. Group dynamics and motivations can vary on many levels. Participants will learn how those factors affect facilitation. They will use tips shared in this session to practice re-engaging the audience through dialogue, feedback, and testing for consensus and understanding.

Training vs. facilitating vs. presenting

- Icebreakers
- Training Rainbow
- Teaching Style Tips
- Presenting and Demonstrating
- Teaching/Socratic Direction
- Facilitating discussion/brainstorming/increasing participation
- Process Monitoring

Unit 5 - Fruitful Feedback

This Unit finishes with an important but sometimes forgotten skill of how to give and receive feedback. During an activity called What Would You Say? Participants evaluate their presentations and also do a peer evaluation and create an action plan on the following areas.

- Relevance of Content
- Level of Content
- Rating of the Presenters
- Knowledge Transfer
- Most Useful Aspect of the Course
- Least Useful Aspect of the Course
- Action plan to go from Fabulous to Fantastic

METHODOLOGY	**ASSESSMENTS**
- Case Studies - Demonstration - Presentations - Expert lectures - Writing and Audio-visual lessons	- Online assignments - Individual and Group

Suggested Books

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
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3.	No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded System Applications Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 0:0:3	SEE Marks : -	Course Code: **P26PC211EC**
Credits : 2	CIE Marks : 50	Duration of SEE : -

Course Objectives	Course Outcomes
1. To Develop the Embedded applications using sensors 2. To learn the interfacing with motors and memory devices 3. To implement the process management functions in Linux 4. To implement the task scheduling algorithms in RTOS 5. To implement the IPC for RTOS	On completion of the course, students will be able to 1. Design Embedded Systems with C51 target interfacing sensor and transducer for RT applications. 2. Design and implement off-chip memories for embedded systems. 3. Demonstrate host to ARM target communication in embOS RTOS environment. 4. Configure emPower board with embOS and validate different scheduling algorithms. 5. Demonstrate different IPC schemes for multi-tasking in embOS and Linux OS.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	2	2	3	1
CO2	3	1	2	3	1
CO3	3	3	3	3	2
CO4	3	3	3	3	2
CO5	3	3	3	3	2

List of Experiments in RTOS using Embedded – C/C++:

1. Interfacing a sensor with ADC0804.
2. Multi-sensor interfacing with ADC0808.
3. Transducer interfacing with DAC0808 for generating a triangular, sawtooth sinusoidal waveforms.

4. Interfacing & controlling the DC Motor
5. Interfacing & controlling the stepper motor
6. Off-chip EEPROM 2KB/4KB interfacing for storing & retrieving lookup tables.
7. Emboss Real time task creation, Demonstration of Multitasking
8. SRAM interface design (1KB/4KB)
9. Interfacing with Timers & DS1307 RTC.
10. Implementation of fork, wait functions in Linux
11. Round Robin Scheduling of 2 Tasks in RTOS
12. Preemptive Scheduling of 2 Tasks in RTOS
13. IPC between 2 Tasks with Binary Semaphore
14. Mailbox usage for IPC between 2 tasks in RTOS

New / Additional experiments planned:

1. Design a Round Robin with the interrupt driven scheduling in ARM by creating three tasks such that 2 tasks perform IPC with the same priority.
2. Porting of RTOS on Embedded target boards
3. Implementation RTOS scheduling of 3 tasks that has to wait for message Queue in Cortex M4F embOS for UI design.

Suggested tools for use:

1. Hardware Target CPU - Cortex M4F power Segger Board, AT89S52
2. Embedded Software Development - Embedded Studio V3.12a
3. Embedded Debugger - Cortex M4F ARM Jlink
4. RTOS - emboss

The break-up of CIE :

1.	No. of Internal Test	:	1
2.	Max. Marks for each internal tests	:	20
3.	Marks for assessment for day to day evaluation	:	30

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Physical Design Laboratory

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 0:0:3	SEE Marks : -	Course Code: **P26PC221EC**
Credits : 2	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
To Design and simulate basic building blocks of mixed signal IC's and perform full custom design of cells.	On completion of the course, students will be able to 1. Perform floor planning, placement and routing of Adder/Counter. 2. Perform layout and parasitic extraction of Adder/Counter. 3. perform full custom design of basic gates and differential amplifier.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	3	3	-
CO2	3	-	3	3	-
CO3	3	-	3	3	-

Part A

1. Layout of basic gates. (inverter / Nand / NOR, Full custom design).
2. DRC and LVS of basic gates. (inverter / Nand /NOR, Full custom design).
3. Parasitic extraction and Post layout simulation of basic gates. (inverter / Nand / NOR, Full custom design).
4. Floor planning, placement and routing of Adder.
5. Layout and parasitic extraction of Adder.
6. Static timing analysis and power analysis of Adder.
7. Floor planning, placement and routing of Counter.
8. Layout and parasitic extraction of Counter.

9. Static timing analysis and power analysis of Counter.
10. Layout of Differential Amplifier.
11. Parasitic extraction and post Layout simulation of Differential Amplifier.
12. Layout, Parasitic extraction and post layout simulation of 1 bit comparator.

Note: Above experiments are to be carried out using Cadence tools (virtuoso Layout editor, assura, spectre circuit simulator and innovus)

Note: Minimum of ten experiments are to be conducted.

The break-up of CIE :

1. No. of Internal Test	:	1
2. Max. Marks for each internal tests	:	20
3. Marks for assessment for day to day evaluation	:	30

Duration of Internal Test : 3 Hours

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Mini Project with Seminar

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : -	Course Code: **P26PW219EC**
Credits : 2	CIE Marks : 50	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his / her specialization.	On completion of the course, students will be able to 1. Selection of a suitable mini project topic / problem for investigation and presentation. 2. Carryout literature survey and prepare the presentation. 3. Formulating the problem, identify tools and techniques for solving the problems. 4. Clear communication and presentation of the seminar topic. 5. Apply ethical principles in preparation of seminar report.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	1	2	1	1	1
CO2	1	2	1	1	1
CO3	1	2	1	1	1
CO4	1	2	1	1	1
CO5	1	2	1	1	1

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the Mini Project and seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Embedded Systems, VLSI Design and related topics.

Mini Project topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

Syllabus for
M.E. ECE (ES & VLSI Design)
III - SEMESTER

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

High Level Synthesis

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26PE310EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

Course Objectives	Course Outcomes
To expose the students, the basics of FPGA designs and synthesis.	On completion of the course, students will be able to 1. Develop simple arithmetic modules and implement in FPGA .(PO1, PO5) 2. Understand various libraries used in HLS based design (PO2) 3. Apply various coding styles for FPGA synthesis and compare their performance (PO1, PO2) 4. Compare the precision data types in System C and Vivado HLS (PO2, PO3) 5. Synthesize a subsystem design using Vivado HLS and port it in FPGA (PO3, PO5)

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			2		1
CO2			2		1
CO3			2		1
CO4			2		1
CO5			2		1

UNIT – I

Introduction to C-based FPGA Design, Using Vivado HLS HLS UltraFast Design Methodology Managing Interfaces Design Optimization RTL Verification, Exporting the RTL Design

UNIT – II

Introduction to the Vivado HLS C Libraries, Arbitrary Precision Data Types Library, The HLS Stream Library, HLS Math Library, Vivado HLS Video Library, The HLS IP Libraries, HLS Linear Algebra Library.

UNIT – III

Coding Styles: Unsupported C Constructs, The C Test Bench Functions, Loops, Arrays, Data Types. C++ Classes and Templates, Using Assertions, SystemC Synthesis.

UNIT – IV

Command Reference, Graphical User Interface (GUI) Reference, Send Feedback, Interface Synthesis Reference, AXI4 Slave Lite C Driver Reference, Video Functions Reference.

UNIT – V

HLS Linear Algebra Library, C Arbitrary Precision Types, C++ Arbitrary Precision Types, C++ Arbitrary Precision Fixed Point Types, Comparison of SystemC and Vivado HLS Types.

Learning Resources:

2. Andres Takach, Creating C++ IP for High Performance Hardware Implementations of FFTs. DesignsDesignCon2002.
3. Preston A. Jackson, Cy P. Chan, Jonathan E. Scalera, Charles M. Rader, and M. Michael Vai - A Systolic FFT Architecture for Real Time FPGA Systems. MIT Lincoln Laboratory 244 Wood ST, Lexington, MA 02420
4. Vivado Design Suite User Guide and Vivado Design Suite Tutorial for High-Level Synthesis.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Low Power VLSI Design

Professional Elective - IV
SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26PE320EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels 2. Apply leakage control mechanisms to reduce static power consumption in DSM VLSI regime 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Study and apply various software power estimation and optimization techniques for low power VLSI system design 5. Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs	On completion of the course, students will be able to 1. Distinguish the impact of various power reduction techniques at different levels of VLSI Design 2. Identify the sources of power dissipation and apply leakage control techniques to reduce static power consumption in CMOS circuits 3. Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits 4. Analyze different power reduction techniques for VLSI systems at Design time, Run-time and Stand-by modes 5. Employ software power estimation and optimization methods for low power VLSI system design 6. Apply low power circuit and architectural techniques such as capacitance reduction, gated clocking, VDD and Vth scaling, DVS etc in digital systems and SRAM designs

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			2		1
CO2			2		1
CO3			2		1
CO4			2		1
CO5			2		1

UNIT – I

Introduction to Low Power design: Why worry about power – at global and SOC levels, Emerging zero-power applications (WSN), 20 nm scenario, Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels)

Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design – Standby leakage control using transistor stacks, Multiple V_{TH} and dynamic V_{TH} techniques, Supply voltage scaling technique (Ref-1)

UNIT – II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories (Ref-2)

UNIT – III

Power Optimization Techniques – II: Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues (Ref-2) Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power (Ref-3)

UNIT - IV

Low Voltage Low Power Static Random Access memories**:** Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, Loadless CMOS 4T SRAM cell, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,
Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction (Ref-1)

UNIT - V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, Varying the clock speed, varying the V_{DD} of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

Learning Resources:

1. Kiat-Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata McGrawhill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, " Low-Power CMOS VLSI Circuit Design" , Wiley Pub., 2000 (Unit III)
4. Dimitrios Soudris, Christian Piguet and Coastas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002 (Topics beyond Syllabus)
5. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010 (for seminars and assignments)

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3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

System on Chip (SoC) Design

Professional Elective - IV

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE330EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
This course covers the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of system design. The course enables students to apply their knowledge for the design of advanced digital hardware systems with help of FPGA tools. 1. Understand the FPGA hardware architecture and interconnect technologies. 2. Apply the knowledge for the design of digital hardware systems. 3. Implementation of FPGA implementation methodologies with the help of FPGA tools. 4. Block level design verification by writing the test benches. 5. System level design verification by writing the test cases.	On completion of the course, students will be able to 1. Understand design flow of SoC 2. Implement the basic level logic functions in hardware system. 3. Implement the block level and system level IP cores. 4. Writing test benches for block level design verification. 5. Writing test benches for system level design verification.

UNIT - I

Introduction to SoC Design, constituents of SoC, Application areas of SoC, SoC development life cycle FPGA architectures for implementing SoC design, FPGA based SoC design flow.

UNIT - II

Front End Design and Back-End Design Overview, Programmable system on chip design, Design with Xilinx zynq SoC platform, Implementation examples of logic functions using LUTs and CLBs, Finite state machine design examples.

UNIT - III

Introduction to IP cores, Block level design using IP cores, Implementation of Block RAM using IP cores, FIFO design and implementation using IP cores.

UNIT - IV

Block Level Design Verification: Introduction to Block-level verification, verification approaches, Functional verification, Static timing verification, Front End Design stages in detail-Flow: Architecture, Design Entry, Simulation, Synthesis and Verification, 16 bit ALU design verification with VIO hardware debugger, Constraints and timings analysis.

UNIT - V

System Level Design Verification: Introduction to system level verification, creating system-level test benches, Applying and migrating test bench-SoC, Design challenges and approaches.

Learning Resources:

1. Veena S. Chakravarthi, "A practical Approach to VLSI System on Chip (SoC) Design", A comprehensive Guide, Springer.
2. Prakash Rashinkar, Peter Paterson and Leena Singh "System-on-a-Chip Verification – Methodology and Techniques", Kluwer Academic Publishers.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
2.	No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

IoT Architectures and Applications

(Professional Elective-V)
SYLLABUS FOR M.E. III – SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE340EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The purpose of this course is to impart knowledge on IoT Architecture, practical constrains, various protocols and multiple case studies.	On completion of the course, students will be able to 1. Understand the Architectural Overview of IoT 2. Enumerate the need and the challenges in Real World Design Constraints 3. Choose the required protocol for a given application. 4. Explore IoT usage in various applications 5. Understand the Security requirements in IoT.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			3		
CO2			3		
CO3			3		
CO4			3		
CO5			3		

UNIT - I : IoT
Definition and Technologies that led to evolution of IOT, Characteristics of IoT, Physical Design of IoT, Logical Design of IoT, IoT Enabling Technologies, IoT Levels & Deployment. M2M and IoT Technology Fundamentals- Devices and gateways, Introduction to cloud IOT platforms like MS Azure, AWS IOT, Google Cloud IOT, Thingworx, Business processes in IoT.

UNIT - II : IoT Reference Architecture
Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. IoT edge system architecture.
Real-World Design Constraints: Technical Design constraints, Connectivity constraints, Data representation and visualization, Big Data Management.

UNIT - III : IoT communications
Data link and physical layer Protocols: PHY/MAC Layer (IEEE 802.11, IEEE 802.15), Bluetooth Low Energy, Thread, introduction to Wi-SUN.
Network Layer Protocols: IPv6, 6LoWPAN;
Transport layer protocols: TCP, UDP;
Messaging protocols: Quality of services in MQTT, standards and security in MQTT, CoAP, AMQP.

UNIT - IV : Case Studies

Smart Cities, Smart Homes, Smart Transportation, Smart Healthcare, Precision Agriculture, Connected Vehicles.

IOT in Indian Scenario: i) IOT and Aadhaar ii) IOT for health services. iii) IOT for financial inclusion. iv) IOT for rural empowerment v) India Urban Data Exchange (IUDX).

Industry 4.0: Industrial Internet of Things (IIoT), Reference Architecture, Characteristics of Industry 4.0.

UNIT - V : Securing the Internet of Things

Security Requirements in IoT Architecture - Security in Enabling Technologies, Security Concerns in IoT Applications.

Security Architecture in the Internet of Things - Security Requirements in IoT, Insufficient Authentication/Authorization, Insecure Access Control, Threats to Access Control, Privacy, and Availability, Attacks Specific to IoT. Security and Vulnerabilities – Secrecy & Secret Key Capacity, Authentication/Authorization for Smart Devices, Transport Encryption, Secure Cloud/Web Interface, Secure Software/Firmware, Physical Layer Security.

Learning Resources:

1 Pethuru Raj and Anupama C. Raman, —The Internet of Things: Enabling Technologies, Platforms, and Use Cases", 1st Edition, 2017, CRC Press.
2 David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton, Jerome Henny "IoT Fundamentals: Networking technologies Protocols, and Use Cases for the internet of things", June, 2017, Cisco press.
3 Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, —From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence‖, 1st Edition, 2014, Academic Press.
4 Arshdeep Bahga, Vijay Madisetti, —Internet of Things: A Hands-on Approach‖, Universities Press, 2014.
5 Practical Internet of Things Security (Kindle Edition) by Brian Russell, Drew Van Duren, Packt Publishing, 2016.
6 Securing the Internet of Things Elsevier Authors: Shancang Li Li Da Xu,Paperback ISBN: 9780128044582,Imprint: SyngressPublished Date: 13th January 2017.
7 https://nptel.ac.in/courses/106105166/5
8 https://nptel.ac.in/courses/108108098/4

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	: 2	Max. Marks for each Internal Test	:	30
2. No. of Assignments	: 3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Tests: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Physical Design Automation

Professional Elective - V

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P (Hrs./week) : 3:0:0	SEE Marks : 60	Course Code: **P26PE350EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will develop placement and routing algorithms for VLSI Designs using C / C++.	On completion of the course, students will be able to 1. understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology. 2. adapt the design algorithms to meet the critical design parameters. 3. map various layout optimization techniques to the algorithms. 4. develop proto-type EDA tool and test its efficacy.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	1		2		
CO2	1		2		
CO3	1		2		
CO4	1		2		

UNIT-I : VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT-II: Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and
Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

UNIT-III: Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

UNIT-IV: Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT-V: Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Learning Resources:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design for Testability

Professional Elective - V
SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26PE360EC**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To expose the students, the basics of testing techniques for circuits.	On completion of the course, students will be able to 1. Illustrate Yield, Fabrication defects, Errors and Faults in VLSI Circuits 2. Simulate digital ICs in the presence of faults and evaluate the given test set for fault coverage. 3. Generate test patterns for detecting single stuck faults in combinational and sequential circuits. 4. Establish a fault model for memory and apply March Tests for fault detection 5. Identify schemes for introducing testability into digital circuits with improved fault coverage. 6. Compare different approaches for introducing BIST into logic circuits, memories and embedded cores.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1			2		1
CO2			2		1
CO3			2		1
CO4			2		1
CO5			2		1

UNIT – I

Introduction: Role of Testing, Digital and Analog VLSI Testing, The Rule of TEN, Yield, Defects and Faults, Reliability and Failure Rate, Test and Design for Testability (DFT)

Modeling: Modeling digital circuits at logic level, register level and structural models.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event- driven simulation. {Ref1: Chs 1,2,3 and Ref2: Ch3)

UNIT – II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence, Fault location and Fault Collapsing, The Single Stuck and Multiple

Stuck Fault Models. Bridging Faults, CMOS Technology Considerations, Intermittent Faults
Fault Simulation: Applications, Fault Simulation for Combinational circuits. (Ref1: Chs 4 and 5)

UNIT – III

Testing for single stuck faults (SSF): Automated Test Pattern Generation (ATPG/ATG) for SSFs in Combinational Circuits, Algorithms (D, PODEM, FAN), ATG for SSFs in Sequential Circuits. Functional Testing without and with Specific Fault Models

Memory Test: Memory density and Defect trends, Faults, Memory Test levels, March Test Notation, Fault Modeling, Memory Testing {Ref1: Chs 6 and 8, Ref2: Ch 9)

UNIT – IV

Design for Testability – Controllability and Observability, AdHoc DFT techniques. Scan architectures and testing – Generic boundary scan, Full Serial integrated scan, Storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – Syndrome test and Signature analysis – LFSR based Signature Analysis (Ref1: Chs 9 and 10)

UNIT – V

Built-in Self-Test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures in brief.

System Test and Core-Based Design: System Test Problem Defined, Functional Test, Diagnostic Test, Testable System design, Core-Based Design and Test –Wrapper, A Test Architecture for SOC, An Integrated Design and Test Approach. {Ref1: Ch 11, Ref2: Ch 18}

DSP-based Analog and Mixed-Signal Test: Functional DSP-based Testing, Static ADC/DAC Testing Methods, CODEC Testing, Dynamic Flash ADC Testing using FFT Technique. {Ref2: Ch 10).

Learning Resources:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
2. Michael L Bushnell and Vishwani D Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits" Kluwer Academic Publishers, 2002
3. NPTEL Course on VLSI Testing – IIT Kharagpur

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Dissertation - Phase - I / Internship

SYLLABUS FOR M.E. ECE (ES&VLSID) - III SEMESTER

L:T:P(Hrs./week): 0:0:20	SEE Marks: -	Course Code: **P26PW319EC**
Credits : 10	CIE Marks: 100	Duration of SEE : -

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his/her specialization	On completion of the course, students will be able to 1. To select the complex engineering problems beneficial to the society and develop solutions with appropriate considerations in the area of VLSI and embedded systems. 2. To apply modern tools and analyze the results to provide valid conclusions. 3. To communicate effectively the solutions with report and presentation following ethics 4. To adapt for the advanced technological changes 5. To work in teams and apply management principles to complete the project economically

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	2			
CO2				3	
CO3			2		
CO4			2		
CO5					3

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry support.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by departmental committee containing of HOD, two senior faculty and supervisor.

Continuous Internal Evaluation (CIE) – 100 marks:

Evaluation Criteria	Maximum Marks
Literature Survey	20
Problem Formulation	20
Design/ Methodology	20
Implementation & Results	20
Presentation & Documentation	20

Note: Rubrics are used for assessment and evaluation.

Syllabus for
M.E. ECE (ES & VLSI Design)
IV - Semester

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Dissertation - Phase - II / Internship

SYLLABUS FOR M.E. ECE (ES&VLSID) - IV SEMESTER

L:T:P(Hrs./week):0:0:32	SEE Marks: -	Course Code: **P26PW419EC**
Credits : 16	CIE Marks: **Viva-Voce Grade**	Duration of SEE:

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of his/her specialization	On completion of the course, students will be able to 1. To select the complex engineering problems beneficial to the society and develop solutions with appropriate considerations in the area of VLSI and embedded systems. 2. To apply modern tools and analyze the results to provide valid conclusions. 3. To communicate effectively the solutions with report and presentation following ethics 4. To adapt for the advanced technological changes 5. To work in teams and apply management principles to complete the project economically

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5
CO1	2	2			
CO2				3	
CO3			2		
CO4			2		
CO5					3

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the 3rd semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

Criteria for Award of Grades:

Academic Performance (%)	Letter Grade	Grade Points
90 to 100	A+ (Outstanding)	10
80 to < 90	A (Excellent)	09
70 to < 80	B+ (Very Good)	08
60 to < 70	B (Good)	07
50 to < 60	C (Average)	06
< 50	F (Fail)	0

Note: Following criteria used for assessment and evaluation.

QUALITY		( )
1.	Review of literature	( )
2.	Scope of the work	( )
3.	Technical soundness (Methodology / Experimental set-up)	( )
4.	Timeliness of work	( )
5.	Conclusions drawn	( )
CONTENT		
6.	Adequacy of data, information and Practical applications / utility	( )
7.	Organization of the thesis	( )
PRESENTATION		
8.	Clear explanation of the work	( )
9.	Justification of work done	( )
10.	Clarity and unambiguity of the language	( )
	Total Score out of 100	( )
(in words_____)		

Open Electives

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Fundamentals of Python Programming

(Open Elective)
SYLLABUS FOR M.E. / M.Tech. II – SEMESTER (Common to all Branches)

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE210CS**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Acquire problem solving skills 2. Write programs using Python language	On completion of the course, students will be able to 1. Develop Python programs with conditional statements and loops. 2. Write programs using functions, strings and lists. 3. Construct Python data structures programs using tuples, dictionaries and set. 4. Write programs using Files. 5. Write programs using Class Concept.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2	PSO3
CO1	1		1	1		1		2
CO2	1	1	1	1	2	1		2
CO3	1	1	1	1	2	2		2
CO4	1	1	1	1	2	2		2
CO5	1		1	1		1		2

UNIT-I:

Basics of Python Programming: Features of Python**,** variables and identifiers, operators and expressions.

Decision control Statements: Selection/Conditional branching statements, basic loop structures/iterative Statements, nested loops, break, continue, and pass Statements.

Functions and Modules: function definition, function call, more on defining functions, recursive functions, modules.

UNIT-II:

Data Structures: Strings: Introduction, built-in string methods and functions, slice operation, String Module. Regular Expressions.

Lists: Introduction, nested list, cloning lists, basic list operations, list methods. Functional programming-filter(),map(),reduce() function.

UNIT –III:

Tuples: Introduction, basic tuple operations, tuple assignment, tuples for returning multiple values, nested tuples, tuple methods and functions.

Set: Introduction, Set operations.

Dictionaries: Basic operations, sorting items, looping over dictionary, nested dictionaries, built-in dictionary functions.

UNIT-IV:

Files and Exceptions: reading and writing files, pickling, handling exceptions. Built-in and user-defined exceptions.

UNIT-V:

OOPS Concepts: Introduction, classes and object, class method and self argument, the_init_()method, class variables and object variables, public and private data members, Inheritance, Operator Overloading.

Learning Resources:

1. Reema Thareja, "Python programming using problem solving approach", Oxford university press.
2. Allen Downey," Think Python: How to Think Like a Computer Scientist", O'Reilly publications, 2nd Edition.
3. Mark Lutz, "Learning Python", O'Reilly Publications.
4. Wesley.J.Chun, "Core Python Programming", Prentice Hall, 2nd Edition.
5. http://www.python.org

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEAPRTMENT OF HUMANITIES AND SOCIAL SCIENCES

Business Analytics

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE210XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Understand the role of business analytics within an organization. 2. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization. 3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making. 4. To become familiar with processes needed to develop, report, and analyze business data. 5. Use decision-making tools/Operations research techniques. 6. Mange business process using analytical and management tools. 7. Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.	On completion of the course, students will be able to 1. Students will demonstrate knowledge of data analytics. 2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics. 3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making. 4. Students will demonstrate the ability to translate data into clear, actionable insights

UNIT -I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT - II

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business

Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT – III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization

UNIT – IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT – V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

UNIT – VI

Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Learning Resources:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 2	Max. Marks for each Internal Tests	:	30
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3.	No. of Quizzes	: 3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
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IBRAHIMBAGH, HYDERABAD – 500 031

DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Industrial Safety

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE220XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT – I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment. Model Curriculum of Engineering & Technology PG Courses [Volume -II] 295

UNIT - III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,

v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Learning Resources:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

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DEPARTMENT OF MECHANICAL ENGINEERING

Operations Research

Open Elective

SYLLABUS FOR M.E. II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE230XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
The objective of this course is to: understand Linear & non-linear programming, transportation modelling , CPM & PERT for project scheduling and control, replacement, game theory and sequencing	On completion of the course, the student will be able to: 1. understand simplex, dual simplex, Sensitivity and transportation and their applications for shop floor problems. 2. understand the importance of Sensitivity analysis and various advanced LPP techniques 3. apply the techniques like CPM and PERT for project management. 4. apply various replacement techniques to find optimum replacement time period for equipment. 5. identify the best strategy to win the game and optimum sequence for minimum elapsed time.

UNIT-I: OPERATIONS RESEARCH-AN OVERVIEW

Meaning and Origin of Operations research, Introduction to Linear programming problems (LPP) -Formulation of LPP-Solution to LPP by Graphical method and simplex method.

UNIT-II: ADVANCED TOPICS IN LINEAR PROGRAMMING

Dual simplex method, special cases in LPP, Duality in LPP, Differences between primal and dual, shadow prices, sensitivity analysis. Non linear programming Khun Tucker conditions.

UNIT-III

Transportation Model: Definition of the transportation model-matrix of Transportation model-Formulation and solution of transportation models-Methods for calculating Initial basic feasible solution, optimal solution by Stepping stone method and MODI method.

Assignment Problem: Hungarian method of assignment problem, maximization in assignment problem, unbalanced problem, problems with restrictions, travelling salesman problems.

UNIT-IV: PROJECT SCHEDULING

Introduction to network analysis, Rules to draw network diagram, Fulkerson rule for numbering events, Critical path method, Summarisation of CPM calculations. PERT, Estimation of probability and its corresponding duration in PERT, Crashing of project and finding of optimal project duration in crashing.

UNIT-V

Replacement models: Introduction, replacement of items that deteriorate ignoring change in money value, replacement of items that deteriorate considering change in money value with time, replacement of items that fail suddenly – individual replacement policy, group replacement policy.

Game theory: Introduction, 2 person zero sum games, maximi– minima principle, principle of dominance, solution for mixed strategy problems graphical method for 2 x n and m x 2 games

Sequencing models: introduction, general assumptions, processing to jobs through 2 machines, processing 'n' jobs through m machines processing 2 jobs through m machines.

Learning Resources:

1. S. D.Sharma, "Operations Research", 10th edition, Newage India Pvt Ltd, New Delhi
2. Hamady.A.Taha An Introduction to Operations Research, "8th edition, TMH
3. Prem Kumar Gupta and Dr. DS Hira, "Operations Research ", S.Chand & Company Pvt. Ltd., 2014.
4. R. Paneerselvam, "Operations Research", PHI Learning Pvt Ltd., 2009.
5. NVS Raju, "Optimization methods for Engineers ", PHI Learning Pvt. Ltd. ., 2014
6. Col D.S. Cheema, "Operations Research", University science press, 2nd edition, India

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests	:	2	Max. Marks for each Internal Tests	:	30
2. No. of Assignments	:	3	Max. Marks for each Assignment	:	5
3. No. of Quizzes	:	3	Max. Marks for each Quiz Test	:	5

Duration of Internal Test: 90 Minutes

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
Accredited by NAAC with 'A++' Grade
IBRAHIMBAGH, HYDERABAD – 500 031

DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Cost Management of Engineering Projects

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE240XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

Introduction and Overview of the Strategic Cost Management Process Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Learning Resources:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Composite Materials

Open Elective

SYLLABUS FOR M.E. - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE250XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT–I

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount

truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Learning Resources:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.
3. Hand Book of Composite Materials-ed-Lubin.
4. Composite Materials – K.K.Chawla.
5. Composite Materials Science and Applications – Deborah D.L. Chung.
6. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

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DEAPRTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Waste to Energy

Open Elective

SYLLABUS FOR M.E. ECE (ES&VLSID) - II SEMESTER

L:T:P(Hrs./week): 3:0:0	SEE Marks : 60	Course Code: **P26OE260XX**
Credits : 3	CIE Marks : 40	Duration of SEE : 3 Hours

UNIT-I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT – III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for Model Curriculum of Engineering & Technology PG Courses [Volume -II] 299 thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT - IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT – V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants –

Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Learning Resources:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

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