VASAVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

ACCREDITED BY NAAC WITH 'A++' GRADE
Ibrahimbagh, Hyderabad-31
Approved by A.I.C.T.E., New Delhi and
Affiliated to Osmania University, Hyderabad-07

Sponsored

by

VASAVI ACADEMY OF EDUCATION

Hyderabad

SCHEME OF INSTRUCTION AND SYLLABI UNDER CBCS FOR

Bachelor of Engineering (ECE)

with

Honours Program in System on Chip Design

With effect from 2026-27
(For the batch admitted in 2024-25)
(R-24)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Phones: +91-40-23146040, 23146041
Fax: +91-40-23146090

Institute Vision

Striving for a symbiosis of technological excellence and human values

Institute Mission

To arm young brains with competitive technology and nurture holistic development of the individuals for a better tomorrow

Department Vision

Striving for excellence in teaching, training and research in the areas of Electronics and Communication Engineering and fostering ethical values

Department Mission

To inculcate a spirit of scientific temper and analytical thinking and train the students in contemporary technologies in Electronics and Communication Engineering to meet the needs of the industry and society with ethical values

B.E (ECE) Honours Program in System on Chip Design Program Educational Objectives (PEO's) Graduates will be able to	
PEO I	Design of FPGA-based digital systems, leveraging hardware description languages, and modern EDA tools to deliver innovative and efficient Engineering solutions
PEO II	Analyze, design, and implement System-on-Chip solutions enabling them to contribute to cutting-edge Embedded systems, VLSI, and Semiconductor industries.
PEO III	Write test benches for system level functional verification of SoCs using different verification methodologies, techniques and EDA tools.

B.E. (ECE) PROGRAM OUTCOMES (PO's) Engineering Graduates will be able to:	
PO1	Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO2	Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO3	Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal and environmental considerations.
PO4	Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
PO11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Lifelong learning: Recognize the need, and for have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS) :: IBRAHIMBAGH, HYDERABAD – 500 031.
ACCREDITED BY NAAC WITH 'A++' GRADE
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHEME OF INSTRUCTION AND EXAMINATION **(R-24)**

Bachelor of Engineering (ECE) with Honours Degree in System on Chip Design

B.E (ECE) Honours Degree in SoC Design										
S. No.	Course Code	Name of the Course	Scheme of Instruction			Scheme of Examination			Credits	Semester
			Hours per Week			Duration in Hrs	Maximum Marks			
			L	T	P		SEE	CIE		
1	U24PC550EC	FPGA Based System Design	3	-	-	3	60	40	**3**	V
2	U24PC551EC	FPGA Based System Design Lab	-	-	2	3	50	30	**1**	V
3	U24PC650EC	SoC Verification Methodologies	3	-	-	3	60	40	**3**	VI
4	U24PC651EC	SoC Verification Methodologies Lab	-	-	2	3	50	30	**1**	VI
5	U24PC740EC	Design Verification	3	-	-	3	60	40	**3**	VII
6	U24PC741EC	Design Verification Lab	-	-	2	3	50	30	**1**	VII
7	U24PW729EC	Course Project	-	-	6	3	50	50	**3**	VII
8	NPTEL Courses: SoC related 1 NPTEL course with 12 weeks duration		-	-	-	-	-	-	**3**	V to VII
		Total	**9**	**-**	**12**		**380**	**260**	**18**	
		Grand Total	**21**				**640**			

Note: Students willing to Opt B.E (ECE) Honours Degree in System on Chip Design shall complete one NPTEL Course Certification (equivalent to 2 Credits weightage) by the end of IV-Semester.

NPTEL Courses Recommended by the ECE Department (R-24)

S.No.	Title	Instructor	Name of the College	Duration
1	Embedded System Design with ARM	Prof. Indranil Sengupta Prof. Kamalika Dutta	IIT Kharagpur	12 weeks
2	Digital VLSI Testing	Prof. Santanu Chattopadhyay	IIT Kharagpur	12 weeks
3	Analog IC Design	Dr. Nagendra Krishnapura	IIT Madras	12 weeks
4	CMOS Analog VLSI Design	Prof. A.N. Chandorkar	IIT Bombay	12 weeks
5	VLSI Physical Design	Prof. Indranil Sengupta	IIT Kharagpur	12 weeks
6	VLSI Design Verification and Test	Dr. Santosh Biswas Prof. Jatindra Kumar Deka	IIT Guwahati	12 weeks
7	C-Based VLSI Design	Prof. Chandan Karfa	IITG	12 Weeks

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FPGA Based System Design

SYLLABUS FOR B.E. (ECE) V - SEMESTER

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: **U24PC550EC**
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To impart foundational understanding of digital circuit design, including combinational and sequential circuits, and critical timing parameters such as setup/hold time, clock skew, jitter, and propagation delay, essential for high-performance system design. 2. To develop proficiency in Verilog HDL for modeling and simulating digital systems, focusing on both blocking/non-blocking assignments and implementation of key digital components such as adders, multipliers, comparators, shift registers, and counters. 3. To enable students to design and implement Finite State Machines (FSMs) using various coding styles (1-always, 2-always, and 3-always blocks) and understand practical aspects of Clock Domain Crossing (CDC), including FIFO design and synchronization techniques. 4. To provide insight into FPGA architecture and hardware modules, introducing students to different FPGA types, I/O modules, internal structures, and design flow, thereby preparing them for real-time embedded system development. 5. To equip students with the skills to design and implement SoC components using Zynq architecture and Verilog HDL, including the use of LUTs, CLBs, and programmable logic blocks, leading to hands-on project development and deployment.	On completion of the course, students will be able to 1. Design and model combinational circuits with Verilog HDL at different levels. 2. Design and analyse various sequential digital circuits by Verilog HDL. 3. Understand the different FSM coding styles and Timing & CDC concepts. 4. Analyse different types of FPGAs and their modules. 5. Understand the Project Design using ZYNQ board.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3										
CO2	2	2	1									
CO3	2	2	1		2							
CO4	2	2	1		2							
CO5	2	2	1		2							

UNIT-I:
Overview of combinational circuits and sequential Circuits, Maximum frequency calculation, set up & Hold time, Clock Skew, Jitter, Propagation Delay, Request load control system.

UNIT-II:
Blocking and nonblocking assignments in Verilog, Verilog Modelling of Combinational Circuits like Adders, Multipliers, Parity Generator Comparators and sequential circuits like Realization of Shift Registers, Realization of a Counter

UNIT-III:
FSM coding styles: Binary, one hot encoding, 1 Always block, 2 Always block, 3 Always block and comparisons among them. FSM based Applications. Clock Domain Crossing, Sync and Async FIFO, FIFO depth calculation.

UNIT-IV:
FPGA general description, Different kinds of FPGA packages, FPGA architecture, Internal hard ware modules of FPGA, their meanings and usage, Basic building blocks, Different kinds of I/0 modules.

UNIT-V:
Zynq Architecture design, Anti fuse, SRAM and EPR0M based FPGAs, Project design using Verilog Hardware Description Language (HDL), Verilog Coding and Simulation of Digital Systems. Implementation examples of Logic functions using LUTs and CLBs.

Learning Resources:

1. Pong P Chu, "FPGA Proto Typing by Verilog Examples" WILEY Publications.
2. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
3. Steve Kilts "Advanced FPGA Design: Architecture, Implementation, and Optimization", WILEY Publications.
4. Verilog HDL: A Guide to Digital Design and Synthesis – by Samir Palnitkar, Prentice Hall PTR Publishers

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FPGA Based System Design Lab

SYLLABUS FOR B.E. (ECE) V-SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: **U24PC551EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
1. To familiarize students with the FPGA design flow using Vivado tools for synthesis, simulation, and hardware implementation. 2. To develop the ability to design, simulate, and implement combinational and sequential digital circuits, including comparators, FSMs, FIFOs, and memory blocks. 3. To train students in creating testbenches for verification and to independently design and implement a digital system through a mini project using HDL.	On completion of the course, students will be able to 1. Learn to write HDL code for simulation and synthesis. 2. Analyse and understand different combinational and Sequential Circuit examples and use the existing examples for new designs. 3. Analyse and understand the timing and utilization for the implemented designs.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3			2							
CO2	2	2			2							
CO3	2	2			2							

List of Experiments:

1. FPGA Design flow using Vivado Tools.
2. Design & Implementation of Combinational Circuit.
3. Design & Implementation of n-bit Comparator.
4. Test Bench Creation and Simulation of Synchronous circuit.
5. Design and Implementation of FSM.
6. Design and Implementation of FIFO.
7. Memory Design and Implementation.
8. Mini Project.

References:

https://reference.digilentinc.com/reference/programmable-logic/zedboard/reference-manual

The break-up of CIE:

1.	No. of Internal Test	:	1
2.	Max. Marks for internal tests	:	12
3.	Marks for day-to-day laboratory class work	:	18

Duration of Internal Test: 3 Hours

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SoC Verification Methodologies

SYLLABUS FOR B.E. (ECE) VI-SEMESTER

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: **U24PC650EC**
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To introduce communication protocols, focusing on the AXI protocol, signal descriptions, and data transaction mechanisms. 2. To familiarize students with System Verilog as an HDVL, including its syntax, data types, and language constructs. 3. To enable students to design testbenches using System Verilog, including concepts like classes, randomization, and verification components. 4. To provide insights into UVM methodology, its structure, components, and advantages over traditional verification approaches. 5. To understand advanced UVM concepts, including phases, TLM, factory usage, objections, and coverage-driven verification	On completion of the course, students will be able to 1. Explain the structure and operation of standard communication protocols, especially AXI, and interpret transaction-level signals and parameters. 2. Apply System Verilog constructs for designing and simulating verification environments, using arrays, queues, strings, and data types. 3. Develop testbenches using object-oriented concepts like classes, random stimulus generation, and modular verification components. 4. Compare traditional and UVM-based verification, and construct reusable testbenches using UVM components and architecture. 5. Implement UVM phases, factory, TLM communication, objection handling, and functional coverage for complete verification workflows.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	2	3							1
CO2	3	2	2	2	3							1
CO3	3	2	2	2	3							1
CO4	3	2	2	2	3							1
CO5	3	2	2	2	3							1

UNIT-I:
Introduction to Protocol, different types of protocol, Intro to AXI Protocol, Basic transaction, Signal description, burst length, size and strobe etc.,

UNIT-II:
System Verilog as a Hardware Design & Verification Language (HDVL); SV language elements, data types, enumeration types, arrays and dynamic arrays, queues, strings.

UNIT-III:
Structures and classes, SV operators and expressions; Transaction class, Randomization of stimulus; generator class, driver class, scoreboard class, monitor class, checker class; Basic testbench in System Verilog.

UNIT-IV:
Introduction to UVM, Directed vs. constrained-random, Comparison of Traditional and UVM Testbenches, UVM objects, UVM Testbench Components, UVM Test bench architecture.

UNIT-V:
UVM Phases and Simulation Flow, UVM Factory and Configuration, TLM Communication, Objection Mechanism, Score boarding and Coverage, Basic UVM Test bench.

Learning Resources:

1. Verilog HDL: A Guide to Digital Design and Synthesis – by Samir Palnitkar, Prentice Hall PTR Publishers.
2. System Verilog for Verification - a guide to learning the Testbench language features; 2nd edition or 3rd edition– by Chris Spear; Springer Verlag Publications.
3. A System Verilog Primer – by J Bhaskar; BS Publications, India.
4. Writing Testbenches – Functional verification of HDL models; 2nd edition by Janick Bergeron; Kluwer Academic Publishers.
5. Universal Verification Methodology UVM Cookbook – by Siemens Digital Industries

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SoC Verification Methodologies Lab

SYLLABUS FOR B.E. (ECE) VI-SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: **U24PC651EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
1. To introduce the use of SystemVerilog data types, arrays, and constraints for effective testbench modeling and verification control. 2. To enable students to build transaction-level SystemVerilog testbenches and verify simple and AXI-based designs. 3. To provide hands-on experience in constructing UVM testbenches using Verification IPs and understanding key UVM components. 4. To develop the ability to design and execute a verification mini-project that applies SystemVerilog/UVM methodologies for real-time protocol or logic verification.	On completion of the course, students will be able to 1. Apply SystemVerilog data types, arrays, and randomization techniques to model and constrain testbench behavior. 2. Develop transaction-level and layered SystemVerilog testbenches for verifying simple DUTs and AXI-based designs. 3. Construct and simulate UVM testbenches using basic Verification IPs and understand the UVM component hierarchy. 4. Design and implement a mini-project demonstrating the verification of a protocol-based or logic-based design using SystemVerilog/UVM methodologies.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	3	2	3				1	1	1	1
CO2	3	2	3	2	3				1	1	1	1
CO3	3	2	3	2	3				1	1	1	1
CO4	3	2	3	2	3				1	1	1	1

List of Experiments for Lab:

1. Exploring System Verilog Data Types and Arrays
2. Building a Transaction-Level Testbench in System Verilog
3. Randomization and Constraints
4. Basic SV Testbench for a Simple DUT

5. Basic UVM Testbench
6. AXI Protocol Transaction Simulation
7. UVM Testbench with Basic VIPs
8. Mini Project.

The break-up of CIE:

1. No. of Internal Test	:	1
2. Max. Marks for internal tests	:	12
3. Marks for day-to-day laboratory class work	:	18

Duration of Internal Test: 3 Hours

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design Verification

SYLLABUS FOR B.E. (ECE) VII-SEMESTER

L:T:P (Hrs/Week): 3:0:0	SEE Marks: 60	Course Code: **U24PC740EC**
Credits: 3	CIE Marks: 40	Duration of SEE: 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
1. To introduce the AXI protocol, its key features, channel types, transaction attributes, and timing diagrams for efficient system communication. 2. To enable students to model and simulate digital components like FIFOs, arbiters, and memory using SystemVerilog, and apply verification techniques including functional coverage. 3. To develop the ability to design AXI-compliant memory modules supporting various burst types and transfer sizes. 4. To train students in building reusable SystemVerilog testbench components and verification agents for AXI protocol-based designs. 5. To impart knowledge of AXI interconnect architecture and its application in connecting multiple AXI agents in complex SoC environments.	On completion of the course, students will be able to 1. acquire knowledge on AXI protocol; should be able to identify and use the AXI transactions. 2. model FIFOs, Arbiter, write test benches and perform code coverage analysis 3. build AXI protocol agents 4. build testbench components using system Verilog 5. learn different AXI interconnect architectures and use AXI interconnect to interface multiple AXI agents.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2		2							
CO2	1	2	2		2							
CO3	2	2	2		2							
CO4	1	2	2	2	2							
CO5	1	2	2	2	2							

UNIT-I:

AXI protocol features and applications; AXI channels; Transaction types and attributes (BURST, SIZE, LENGTH.); narrow transfers; AXI Read and Write Operations Address and control signalling; Data transfer mechanics and handshaking; Example AXI read and write transactions Timing Diagrams Explanation of AXI protocol timing diagrams

UNIT-II:

Modeling of Synchronous and Asynchronous FIFO, Arbiter, Memory model, FSMs using SystemVerilog; writing basic testbench to verify the functionality; Verification coverage – statement-, block-, branch-, expression-, and FSM-coverage. Verification tools and verification plan; Architecting test benches; Writing basic self-checking test benches; role of tasks and functions in test benches; automatic taks and functions; Understanding fork-join execution.

UNIT-III:

Designing Memory with AXI slave interface that supports all burst types, narrow transfers

UNIT-IV:

Developing verification component for AXI Slave verification. Transaction class, Randomization of stimulus; generator class, driver class, scoreboard class, monitor class, checker class.

UNIT-V:

Introduction to AXI Interconnect; Role of AXI interconnect in multi-master/slave systems; Basic building blocks of AXI interconnect; Address decoding, switching, and routing (using cross bar switch)

Learning Resources:

1. http://www.gstitt.ece.ufl.edu/courses/fall15/eel4720_5721/labs/refs/AXI4_specification.pdf
2. System Verilog for Verification – a guide to learning the Testbench language features; 2nd edition or 3rd edition– by Chris Spear; Springer Verlag Publications.
3. A System Verilog Primer – by J Bhaskar; BS Publications, India.
4. Writing Testbenches – Functional verification of HDL models; 2nd edition by Janick Bergeron; Kluwer Academic Publishers

The break-up of CIE : Internal Tests + Assignments + Quizzes

1. No. of Internal Tests : 2 Max. Marks for each Internal Test : 30
2. No. of Assignments : 3 Max. Marks for each Assignment : 10

Duration of Internal Test: 90 Minutes

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Design Verification Lab

SYLLABUS FOR B.E. (ECE) VII-SEMESTER

L:T:P (Hrs./week) : 0:0:2	SEE Marks : 50	Course Code: **U24PC741EC**
Credits : 1	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVE	COURSE OUTCOMES
1. To enable students to develop SystemVerilog models for AXI-based data transfer types including INCR, FIXED, WRAP, and narrow transfers. 2. To train students in designing parameterized memory modules, arbiters, and FIFOs with appropriate control and status flags using SystemVerilog. 3. To impart skills for modeling sequential circuits by designing FSMs, creating block diagrams, and writing corresponding SystemVerilog code for digital system implementation.	On completion of the course, students will be able to 1. Develop system Verilog models for memories and data transfers. 2. Design various sequential circuits using system Verilog. 3. Develop system Verilog models for arbiters.

CO-PO-PSO Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2		3							
CO2	2	2			3							
CO3	2	2	2		3							

Laboratory Experiments:

1. Develop System Verilog model to generate the INCR, FIXED and WRAP transfers.
2. Develop System Verilog model to generate narrow transfers.
3. Develop the parametrized System Verilog model for Single Port and two port memories (ROM and RAM).
4. Develop System Verilog model for Arbiters (Fixed, Round Robin and Weighted Round robin).

5. Develop System Verilog model for Synchronous and Asynchronous FIFO, with FULL, Alomost_full, Empty and Almost Empty, Underflow, overflow flags.
6. Develop Digital block level diagram, FSM and do SystemVerilog code for sequential circuits for general problem statements.

The break-up of CIE:

1.	No. of Internal Test	:	1
2.	Max. Marks for internal tests	:	12
3.	Marks for day-to-day laboratory class work	:	18

Duration of Internal Test: 3 Hours

With effect from the academic year 2026-27

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A++' GRADE
IBRAHIMBAGH, HYDERABAD – 500 031

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Project

SYLLABUS FOR B.E. (ECE) VII-SEMESTER

L:T:P (Hrs./week) : 0:0:6	SEE Marks : 50	Course Code: **U24PW729EC**
Credits : 3	CIE Marks : 50	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design.	On completion of the course, students will be able to 1. To select the complex engineering problems beneficial to the industry & society and develop solutions with appropriate considerations. 2. To apply modern tools and analyze the results to provide valid conclusions. 3. To communicate effectively the solutions with report and presentation following ethics. 4. To work in teams and adapt for the advanced technological changes 5. To apply management principles to complete the project economically

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	3			2	2					
CO2				3	3							
CO3								3		3		
CO4									3			3
CO5											3	

Note: Some of relevant COs must be mapped with the relevant PSOs based on the domain and application area of the project.

Oral presentation is an important aspect of engineering education. The objective of the course project is to prepare the student for a systematic and independent study of the state of the art topics in a broad area of System on Chip Design.

Project topics may be chosen by the student with advice and approval from the faculty members. Students are to be assessed and evaluated as per the following criteria.

Each student is required to:

1. Submit a one-page synopsis in the beginning of project work for display on the notice board.
2. Give a 20 minutes presentation through LCD power point presentation followed by a 10 minutes discussion.
3. Submit a report on the project work with list of references and slides used.

Project reviews are to be scheduled from the 3rd week of the semester to the last week of the semester and any change in schedule should be discouraged.

- Batch size shall be 2 to 3 students.
- Allocation and finalization of the projects by department.
- Two reviews – One during 5th week and another during 10th week and final evaluation shall be conducted during 15th to 16th week.
- Students are required to give Presentations during the reviews.
- Students are required to submit project report.

Continuous Internal Evaluation (CIE) – 50 marks:

Evaluation Criteria	Maximum Marks
Literature Survey	10
Problem Formulation	10
Design/ Methodology	10
Implementation & Results	10
Presentation & Documentation	10

Semester End Examination (SEE) – 50 marks:

Evaluation Criteria	Maximum Marks
Literature Survey	10
Problem Formulation	10
Design/ Methodology	10
Implementation & Results	10
Presentation & Documentation	10

Note: Rubrics are used for assessment and evaluation.